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hardware parallelism & transaction processing systems

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transaction vs. analytical processing

OLTP	OLAP
short-running simple requests	long-running complex requests
access small portion of the data	access lots of data
fetch several columns of a record	fetch a few columns of a record
lookup, insert, delete, update	SQL queries, map-reduce jobs, machine learning, graph analytics, …
deposit money to a customer's account, lookup information about a product, looking up a tweet, …	*customers who are most likely to get mortgages next year, item sold the most last year in each department of a store grouped by months, …*

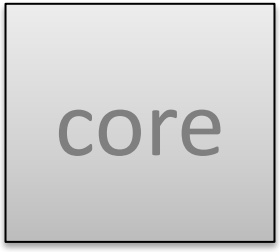
➔ **primary applications for databases**

➔ **required functionality & optimizations differ**

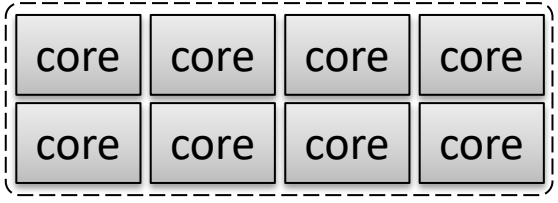
evolution of general-purpose CPU

… the hardware we run transactions on

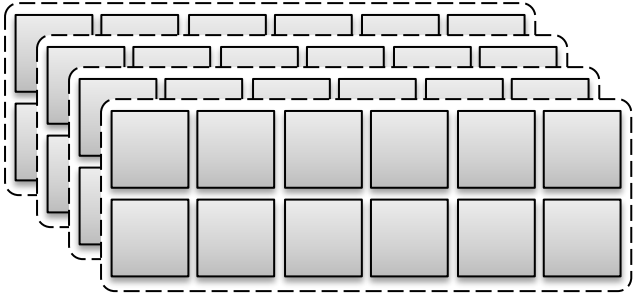
2005



single-core CPUs



multicore CPUs



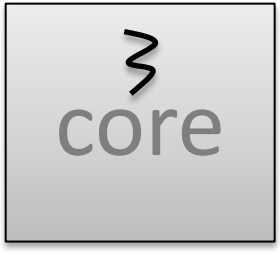
multisocket multicore CPUs

faster & more-complex cores over time

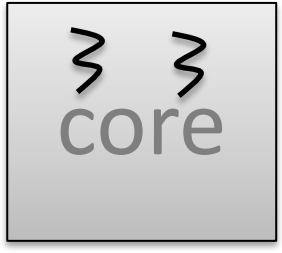
similar speed & complexity in a core, more cores over time

types of hardware parallelism

implicit/vertical parallelism



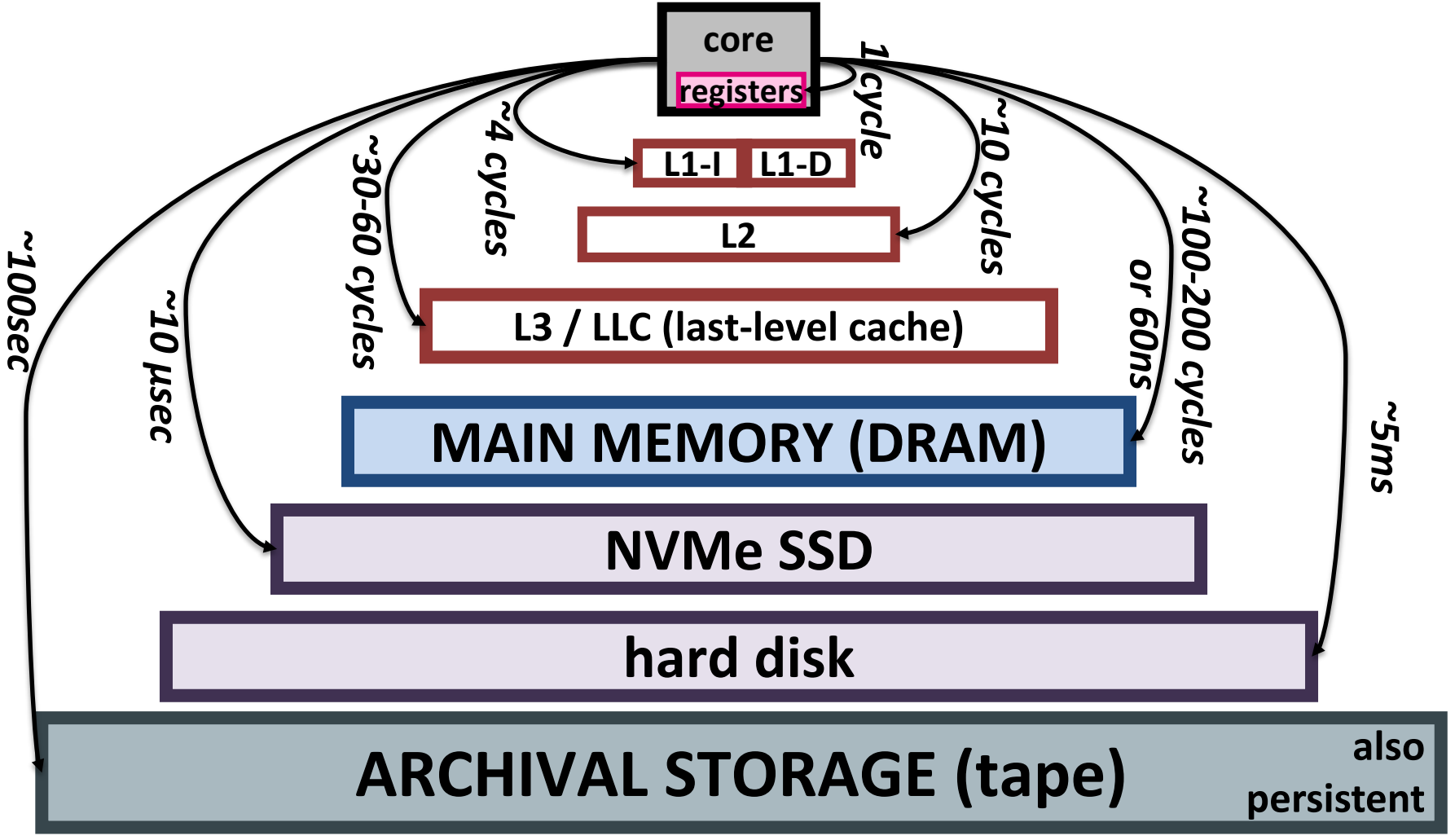
instruction & data parallelism
hardware does this automatically



multithreading
threads share
execution cycles
on the same core

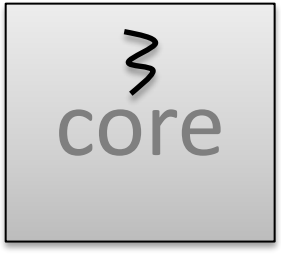
why do we need this?

single-core – access latency to storage

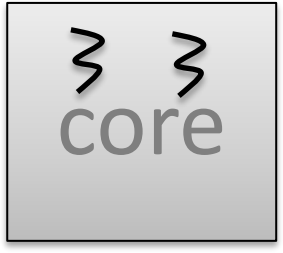


types of hardware parallelism

implicit/vertical parallelism



instruction & data parallelism
hardware does this automatically

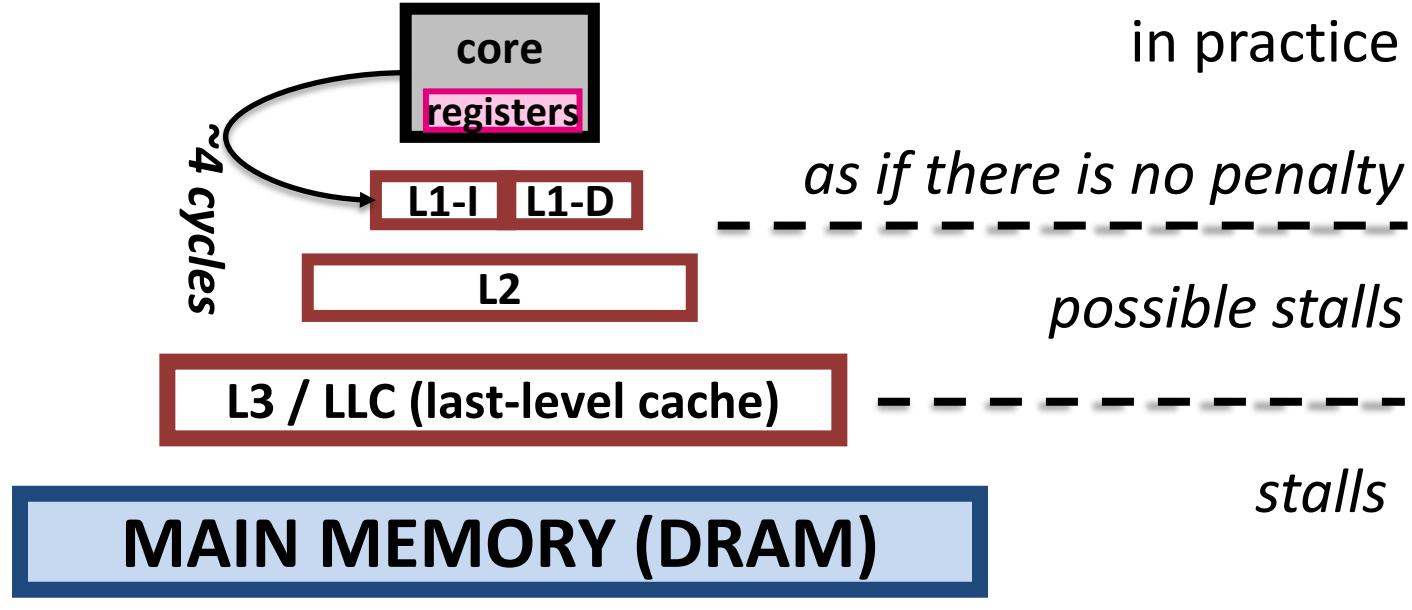


multithreading
threads share
execution cycles
on the same core

why?
we don't want cores to stay idle waiting for instruction/data accesses!

goal: minimize stall time due to cache/memory accesses
overlapping access latency for one item with other work

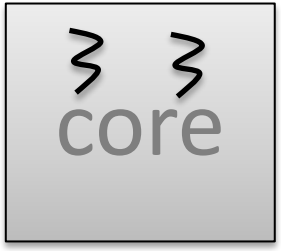
single-core – access latency to storage



stalls = 😴

types of hardware parallelism

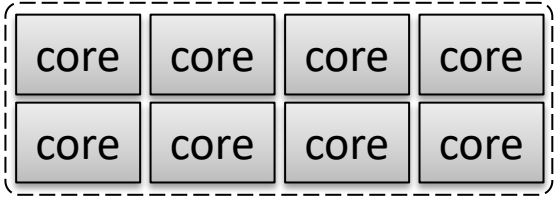
implicit/vertical parallelism ⟷ **explicit/horizontal parallelism**



single-core

instruction & data parallelism

simultaneous multithreading



multicores

multiple threads run in parallel on different cores

why do we have this?

wording courtesy of Wikipedia

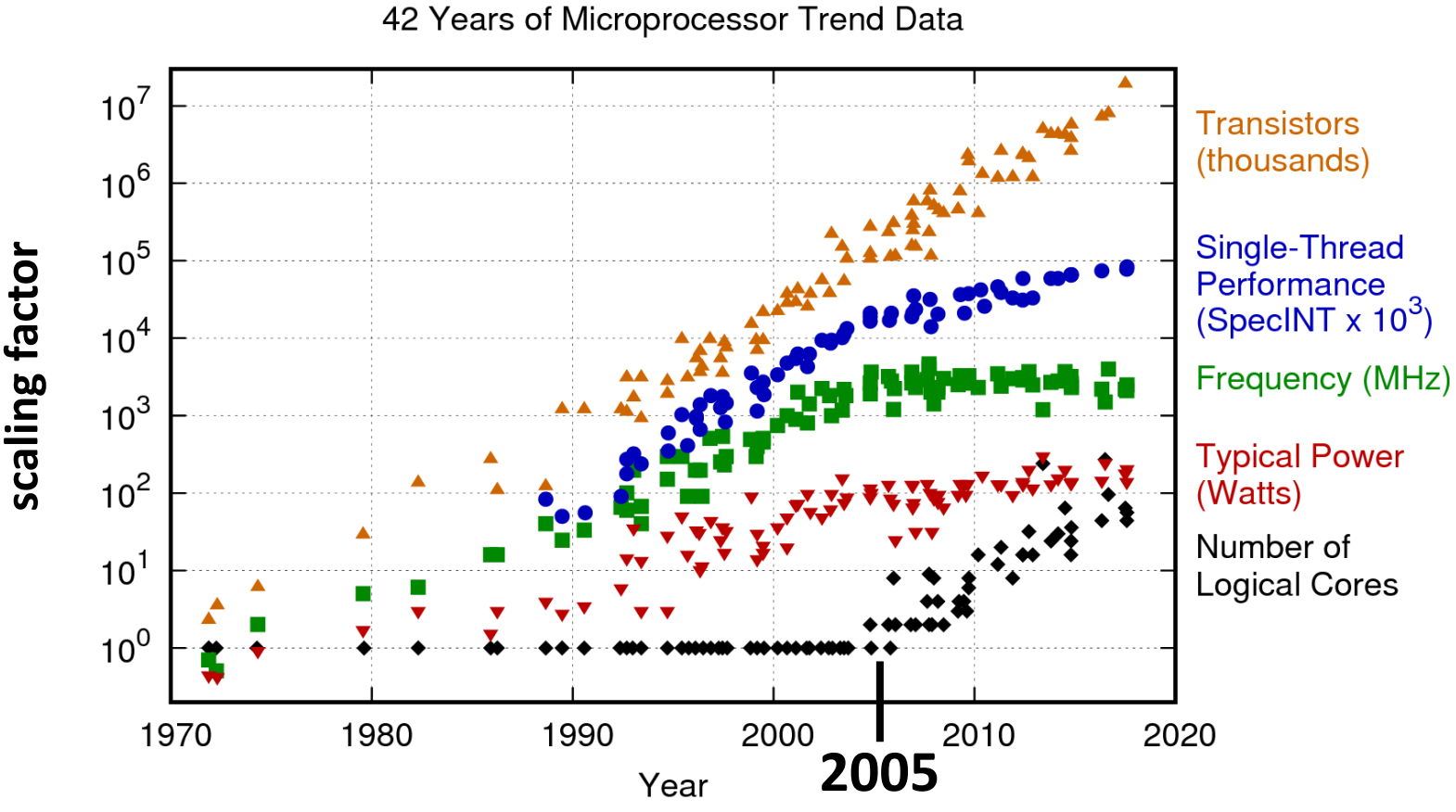
for Moore's law to be practical you need Dennard scaling!

Moore's law

"… the observation that the number of transistors in a dense integrated circuit doubles approximately every two years."

Dennard scaling

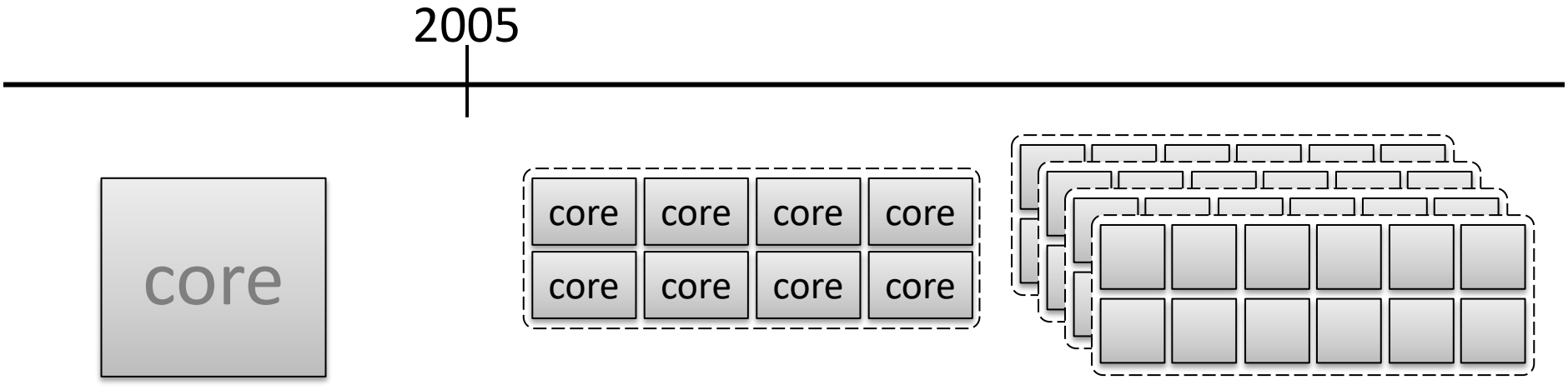
" … as transistors get smaller their power density stays constant, so that the power use stays in proportion with area: both voltage and current scale (downward) with length."



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2017 by K. Rupp

doubling of transistor counts continues
power and clock speeds hit the wall

commodity CPU evolution



single-core CPUs

multicore CPUs

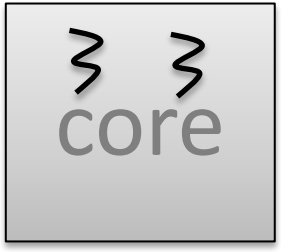
multisocket multicore CPUs

Dennard scaling doesn't hold anymore

switching to multicores kept Moore's Law alive

types of hardware parallelism

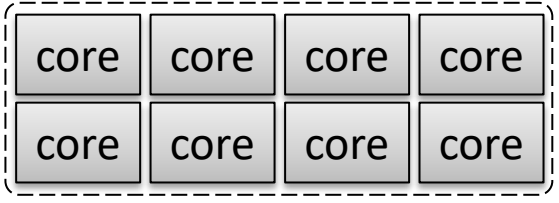
implicit/vertical parallelism ⟷ **explicit/horizontal parallelism**



single-core

instruction & data parallelism

simultaneous multithreading



multicores

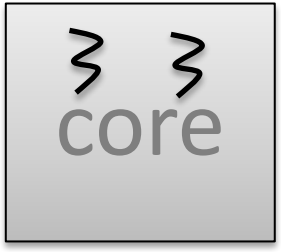
multiple threads run in parallel on different cores

implicit parallelism → (almost) free lunch

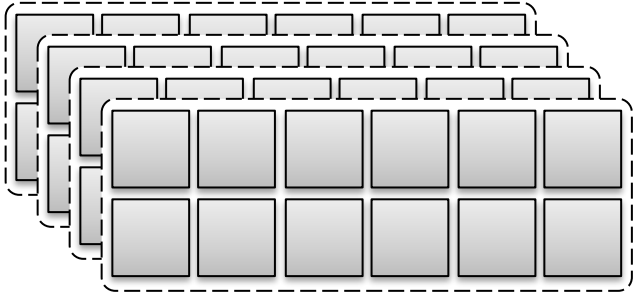
explicit parallelism → must work hard to exploit it

types of hardware parallelism

implicit/vertical parallelism ⟷ **explicit/horizontal parallelism**



single-core
instruction & data parallelism
simultaneous multithreading



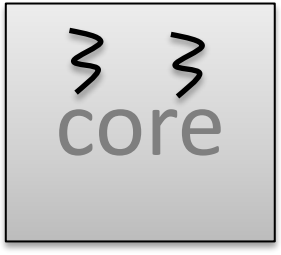
multisocket multicores
multiple processors/CPUs
in one machine

implicit parallelism → (almost) free lunch

explicit parallelism → must work hard to exploit it

types of hardware parallelism

implicit/vertical parallelism ⟷ **explicit/horizontal parallelism**



single-core
instruction & data parallelism
simultaneous multithreading

distributed systems
running a program over
multiple machines

implicit parallelism → (almost) free lunch

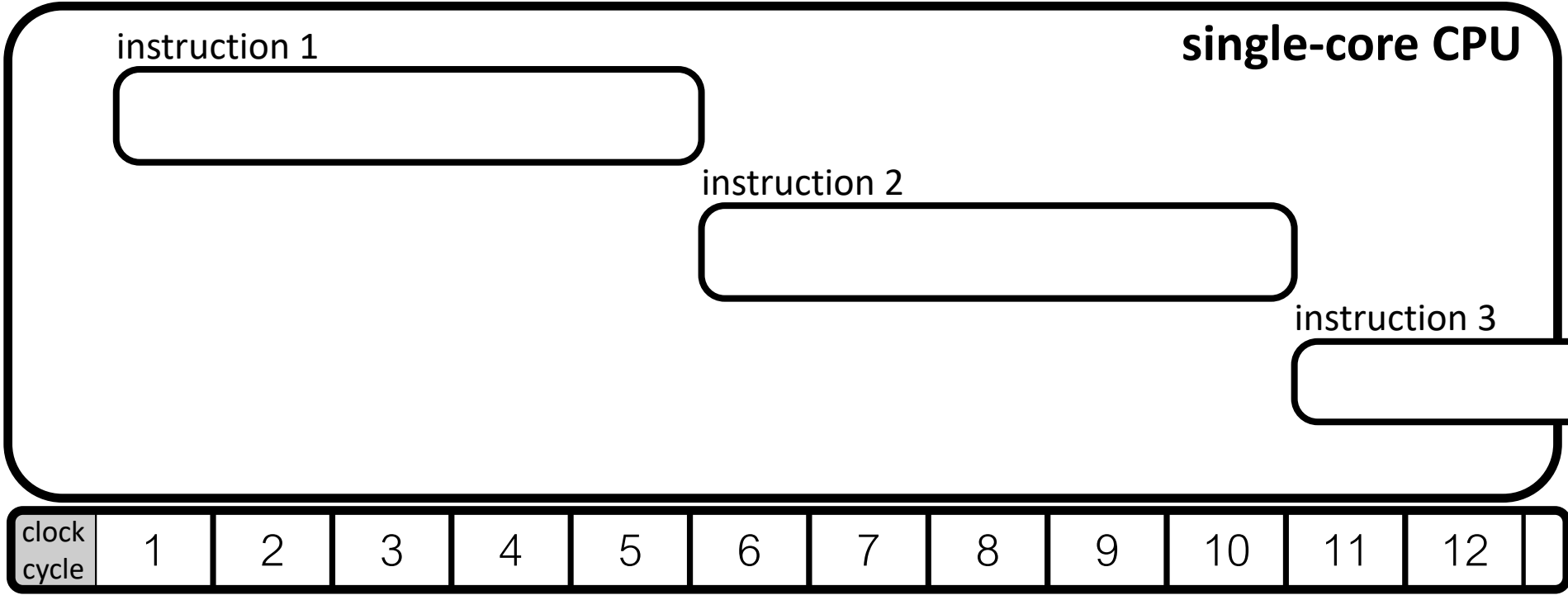
explicit parallelism → must work hard to exploit it

agenda

- types of hardware parallelism
- **implicit parallelism**
- explicit parallelism

subscalar CPU (i.e., no implicit parallelism)

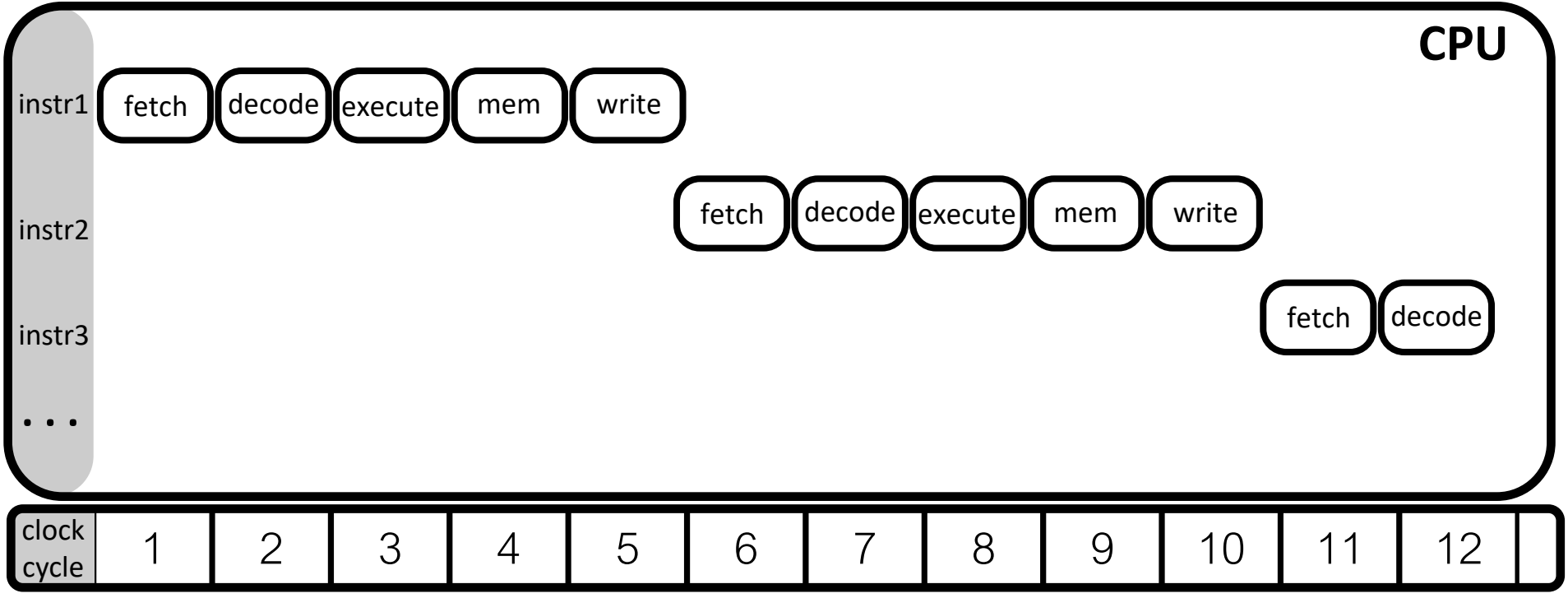
one instruction at a time



several cycles to complete two instructions, assuming no long-latency data/memory accesses

subscalar CPU (i.e., no implicit parallelism)

one instruction at a time



several cycles to complete two instructions, assuming no long-latency data/memory accesses

RISC instruction stages

fetch
the instruction from the cache

decode
specifying which operation the instruction performs and inputs it needs

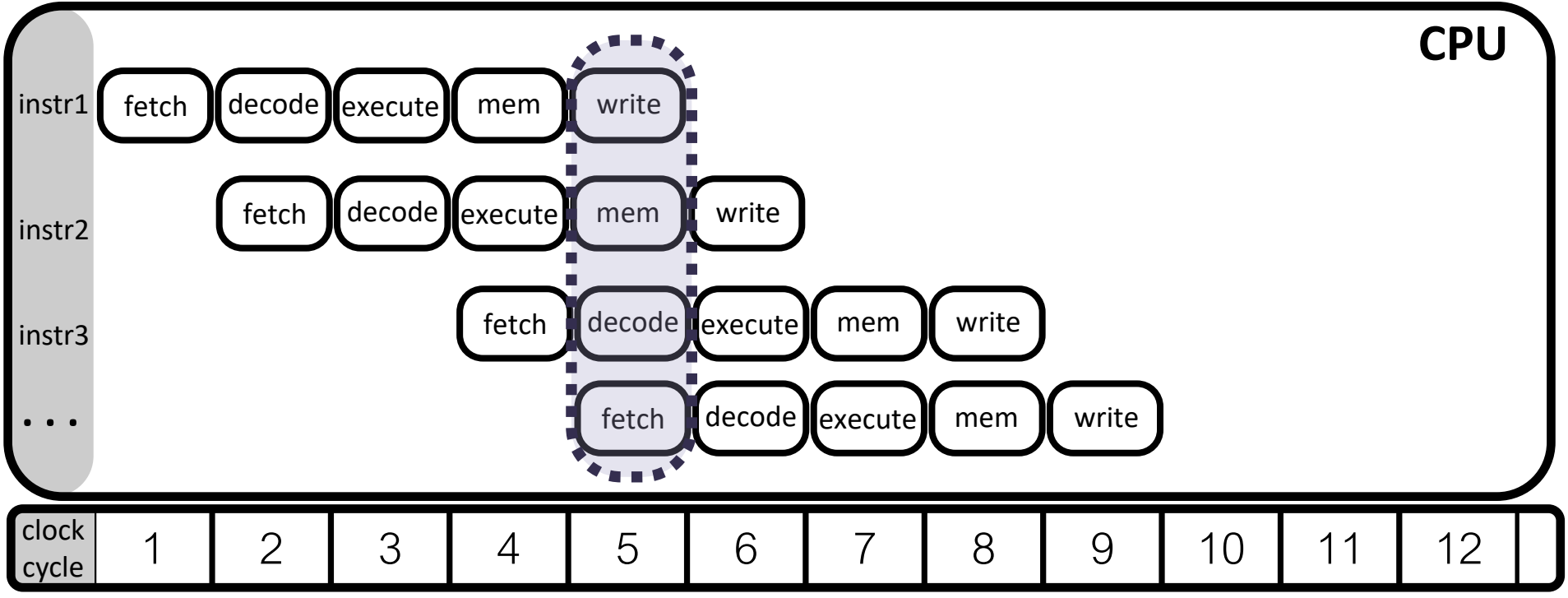
execute
the operation itself

memory
accessing the memory for inputs if needed

write
writing back the results into registers

instruction pipelining

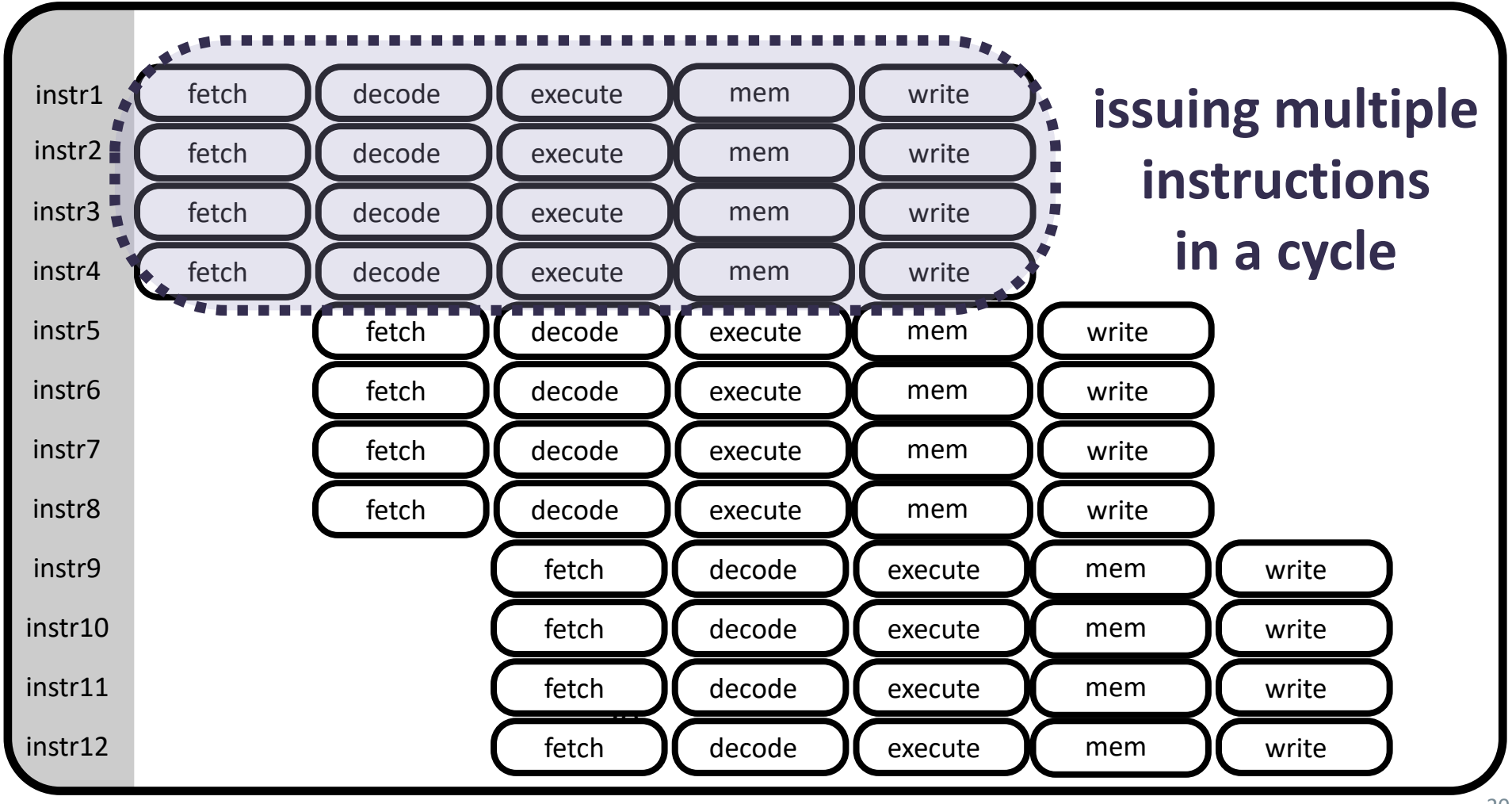
overlapping stages of different instructions



fundamental way to parallelize implicitly

superscalar CPU

example of 4-way superscalar CPU



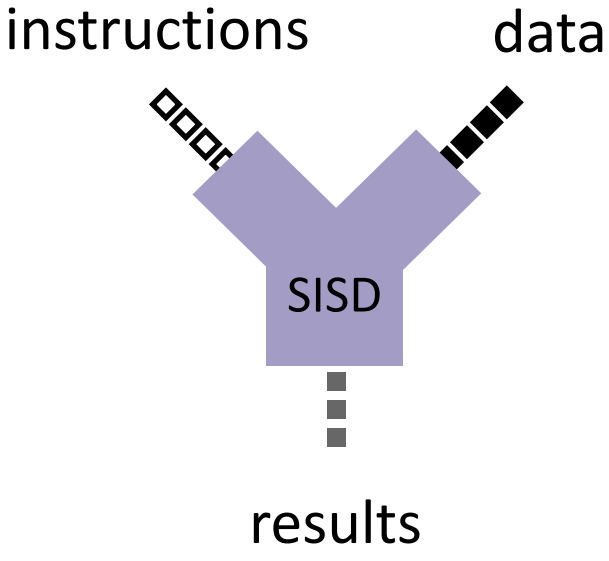
out-of-order (OoO) execution

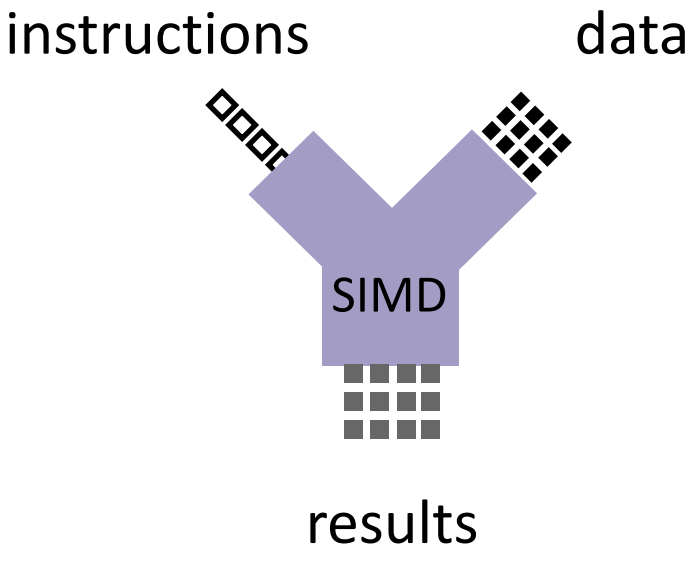
allows a processor to execute instructions based on the availability of input data rather than strictly following the instruction ordering of a program

example:

(1) r1 ← r2 / r3
(2) r4 ← r1 + r5
(3) r6 ← r7 * r8 → **independent from the previous two, can be executed independently in parallel or before 1 & 2**

single instruction multiple data (SIMD)





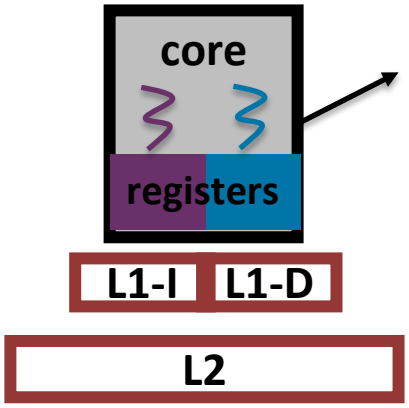
also implicit data parallelism, but this one has to be managed/issued by the software

simultaneous multithreading (SMT)

keep state/context of multiple threads via more register space

each CPU cycle, you swap the thread being executed

OS don't have to do a context switch for this

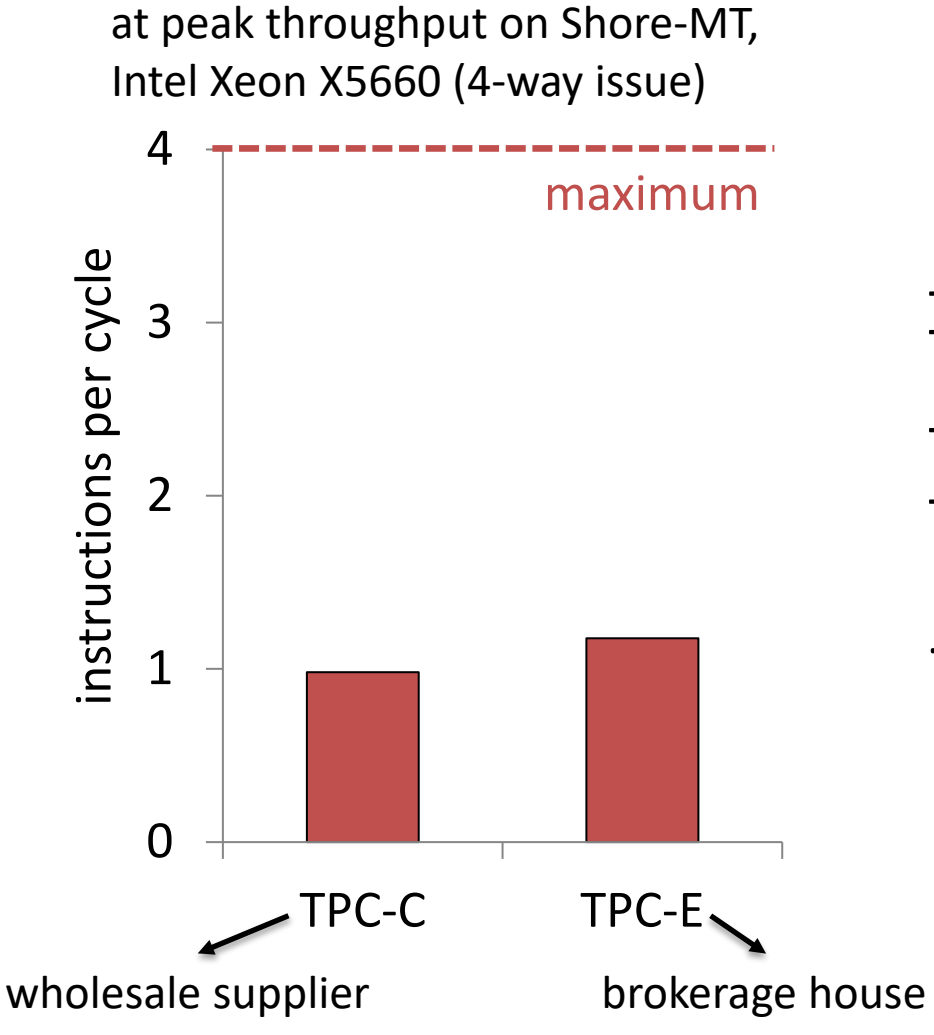


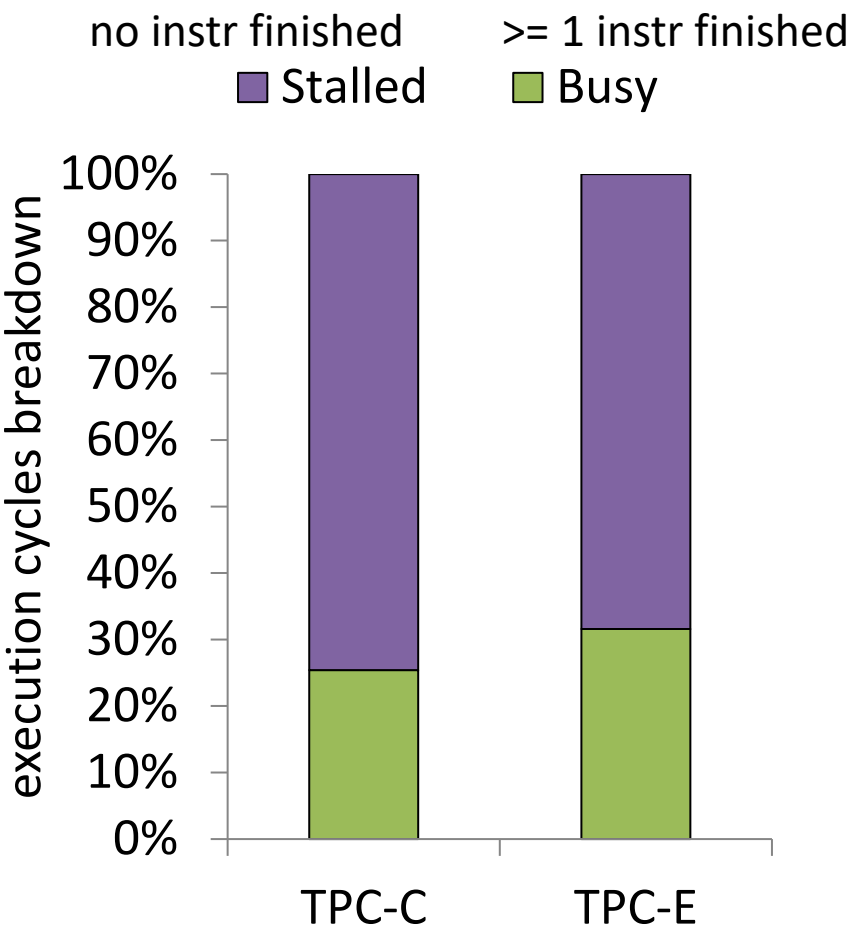
example of a core that supports two hardware contexts or logical threads

more pressure on shared hardware resources (e.g., caches)

if not used right, may not give much benefit or may even hurt performance

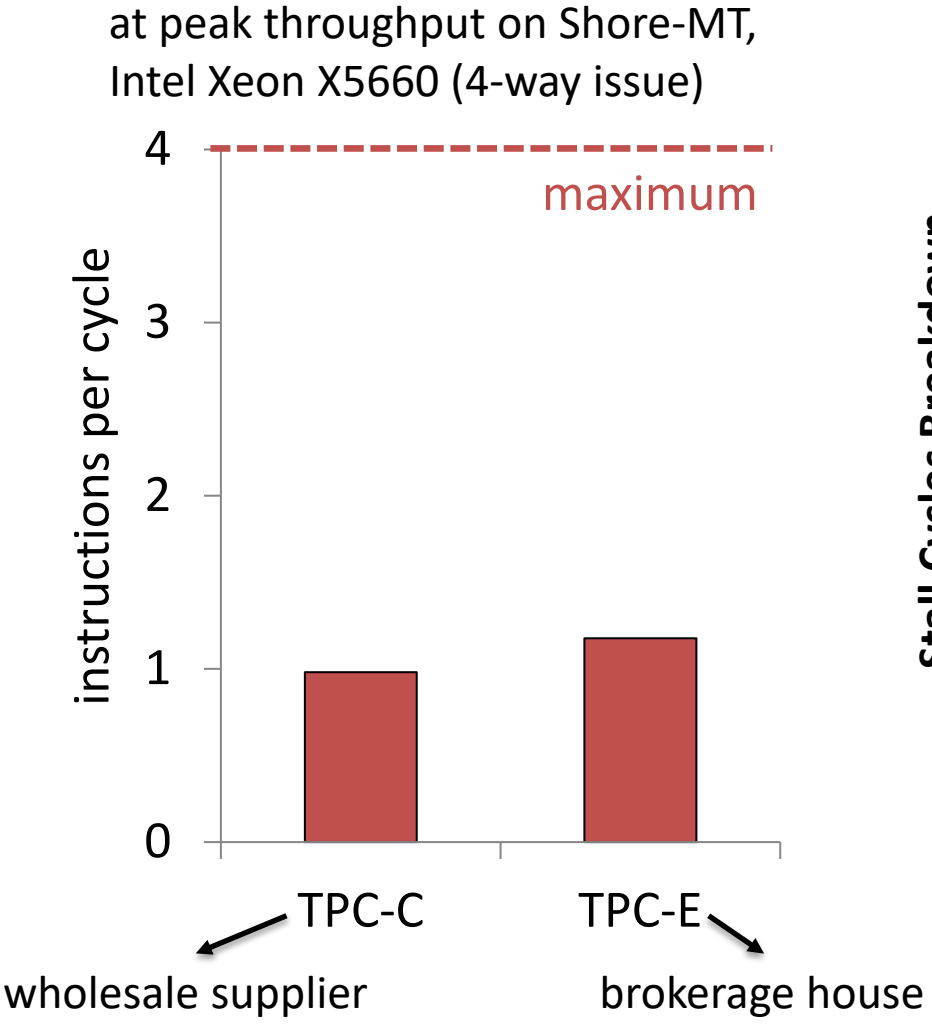
OLTP & implicit parallelism

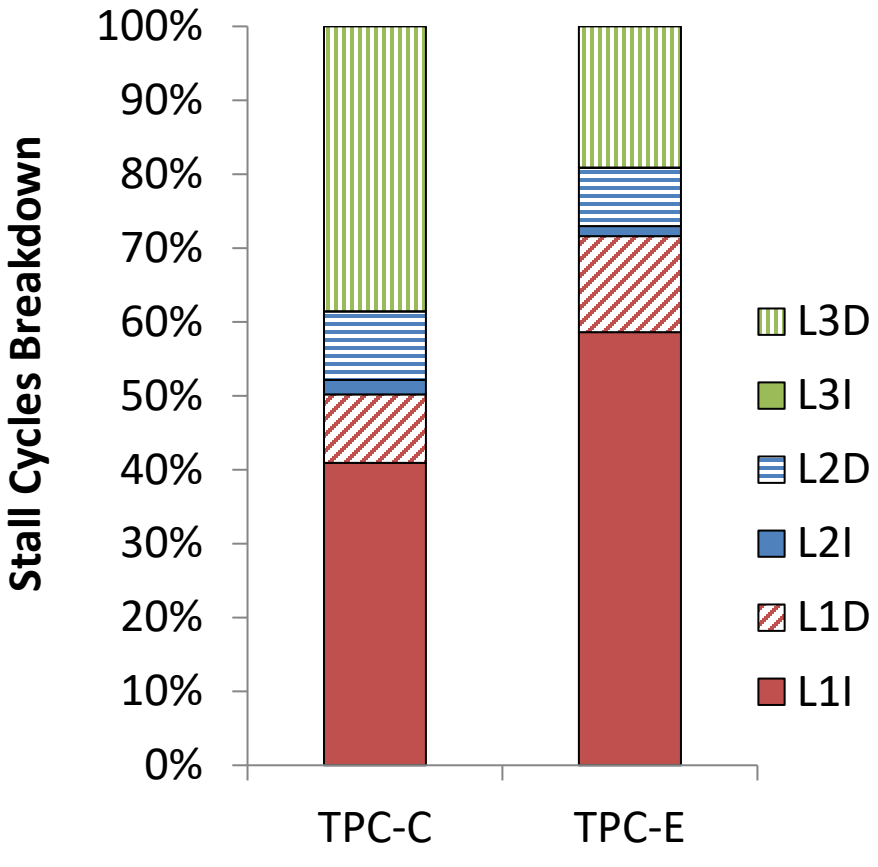




[EDBT13]

OLTP & implicit parallelism

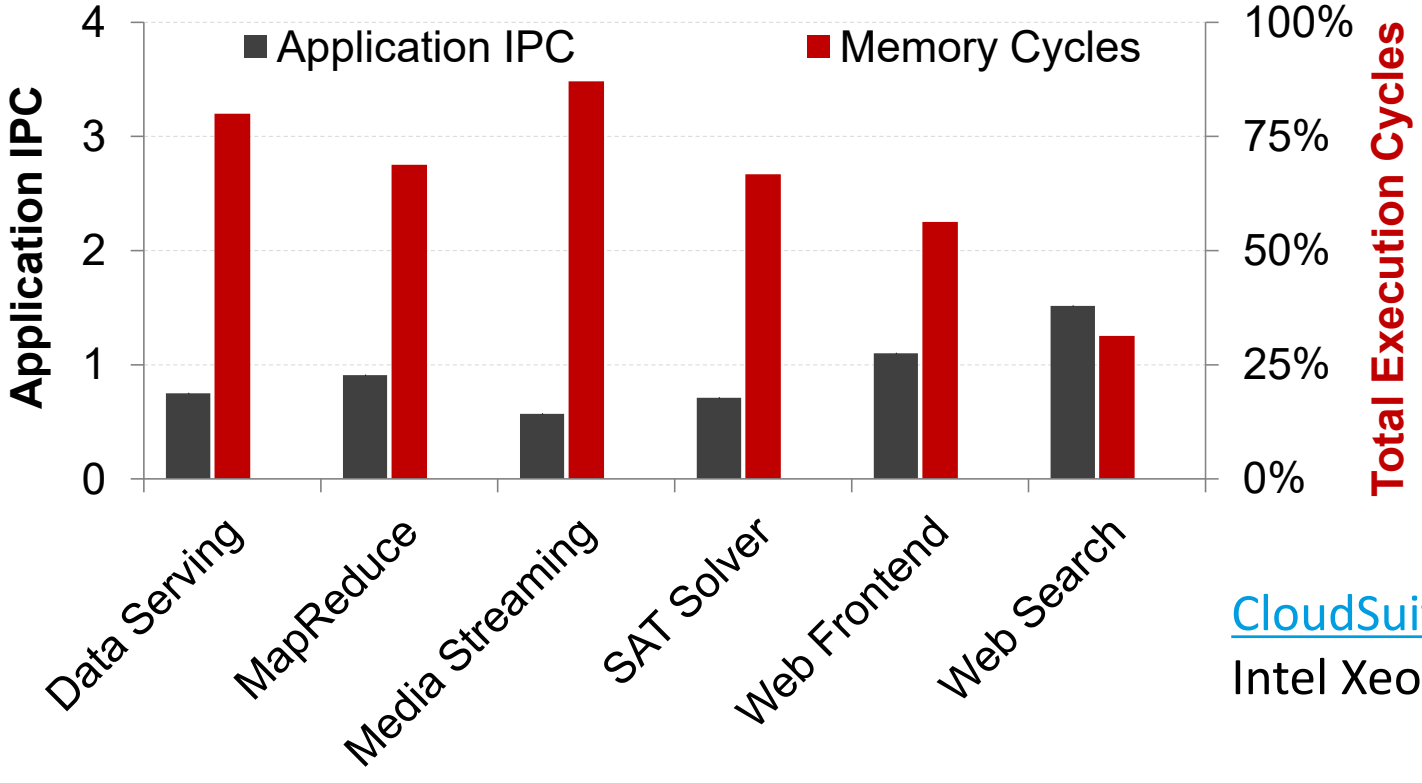




[EDBT13, DaMoN13]

memory stalls in data-intensive apps

[ASPLOS12]

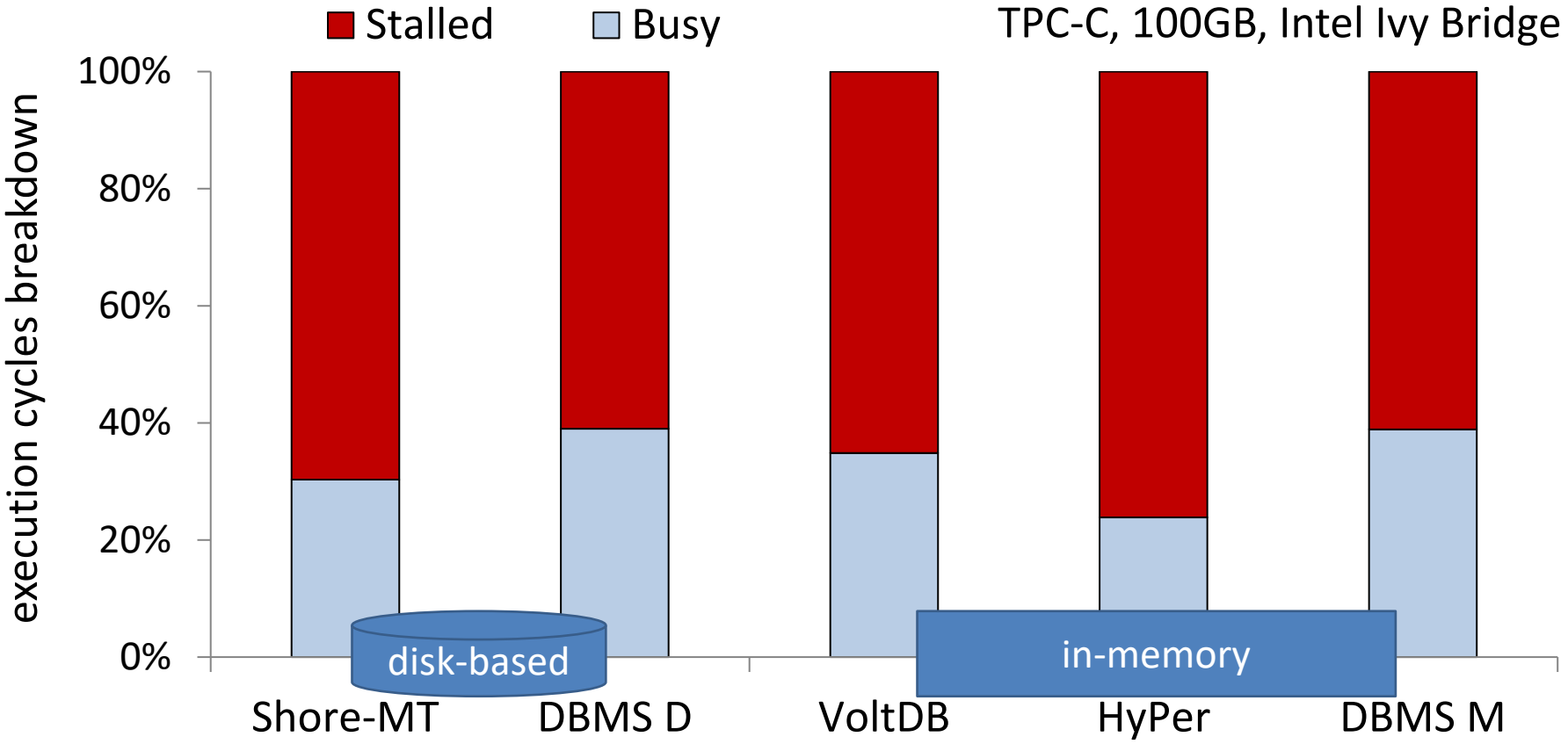


CloudSuite on Intel Xeon X5670

data-intensive apps suffer due to memory stalls not just due to data but also instructions

what about in-memory OLTP?

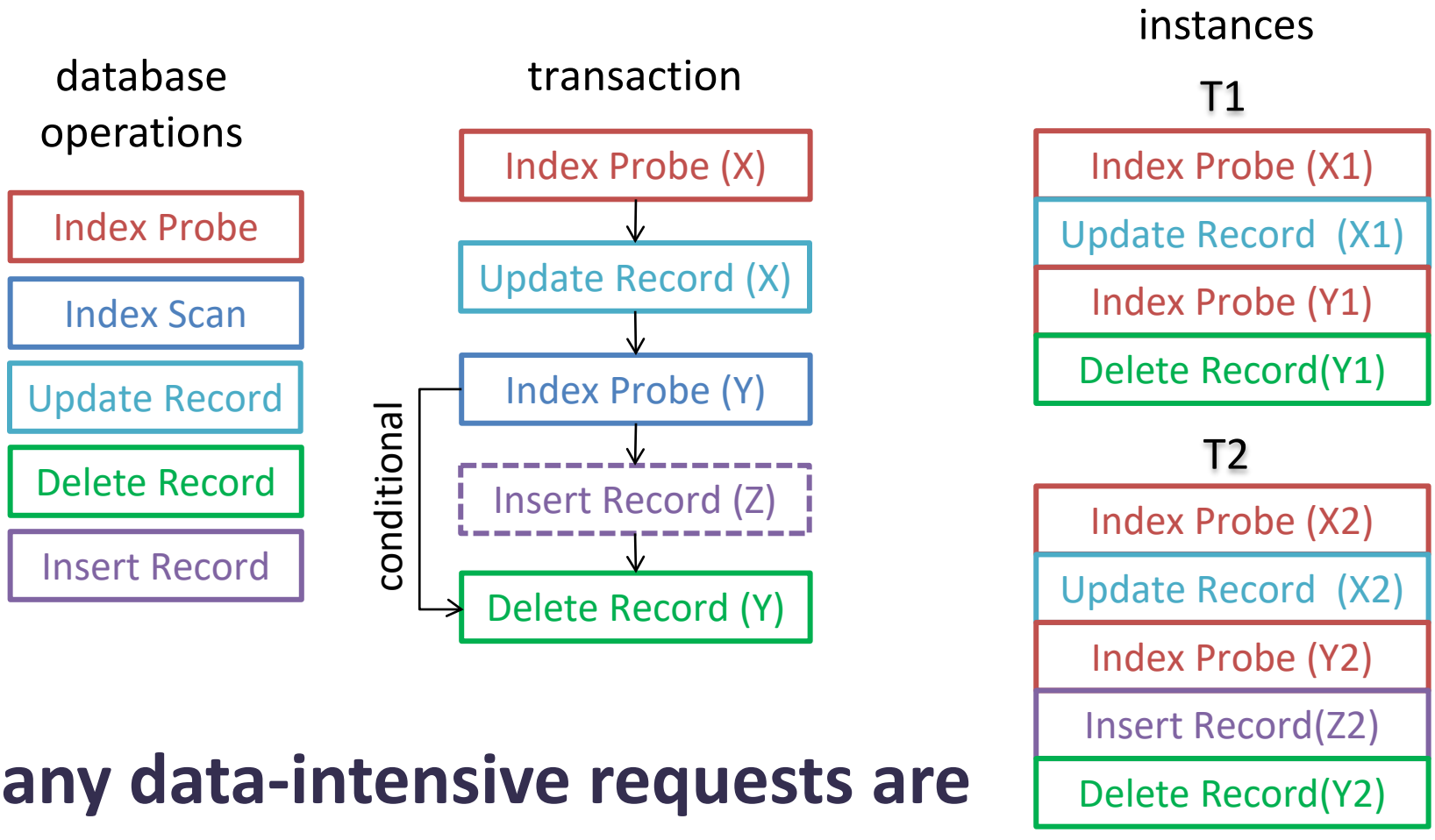
[SIGMOD16]



doesn't mean these systems are bad

it means we are leaving performance on the table

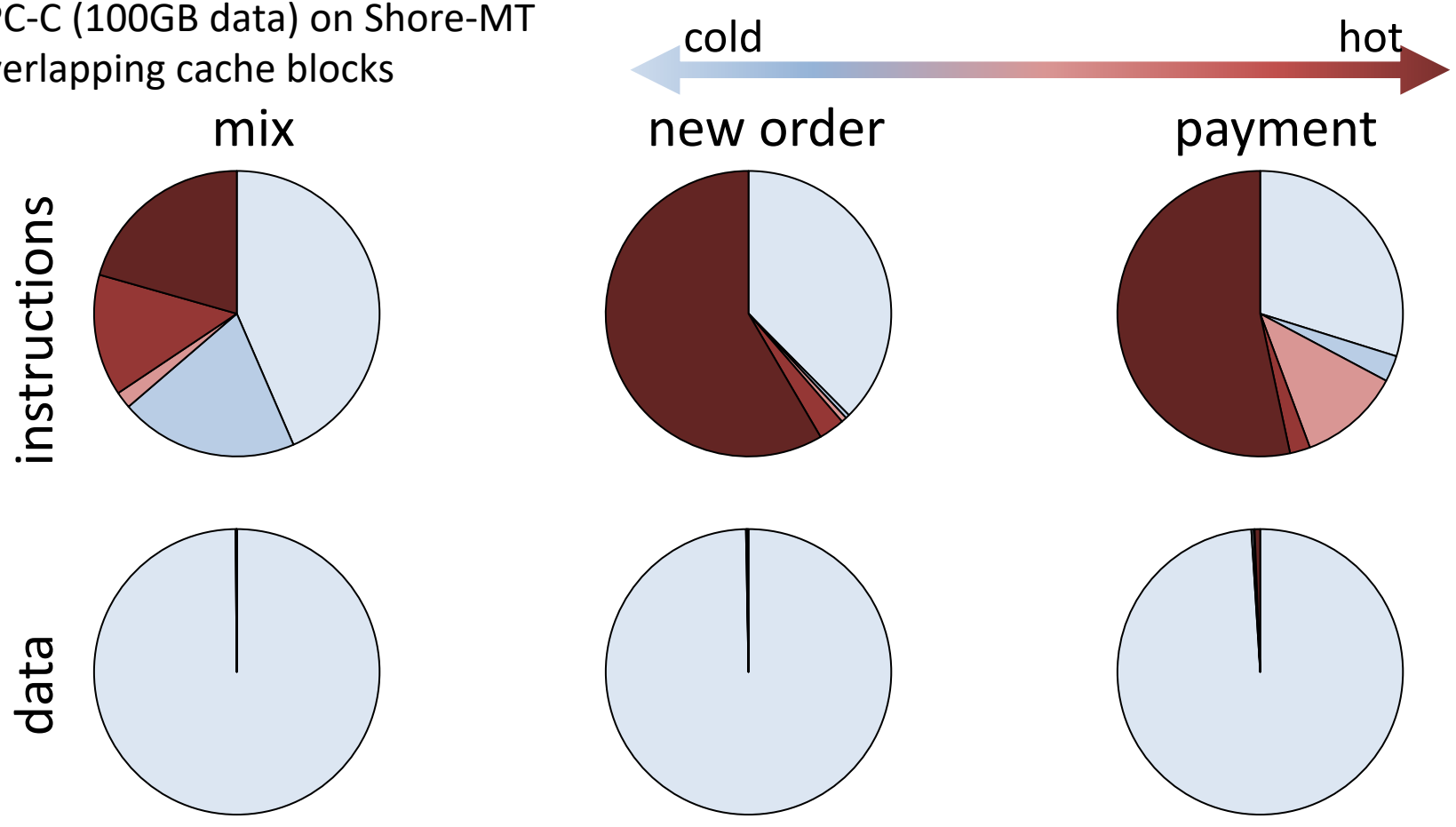
transactions under microscope



many data-intensive requests are composed of common instructions

instruction & data overlap

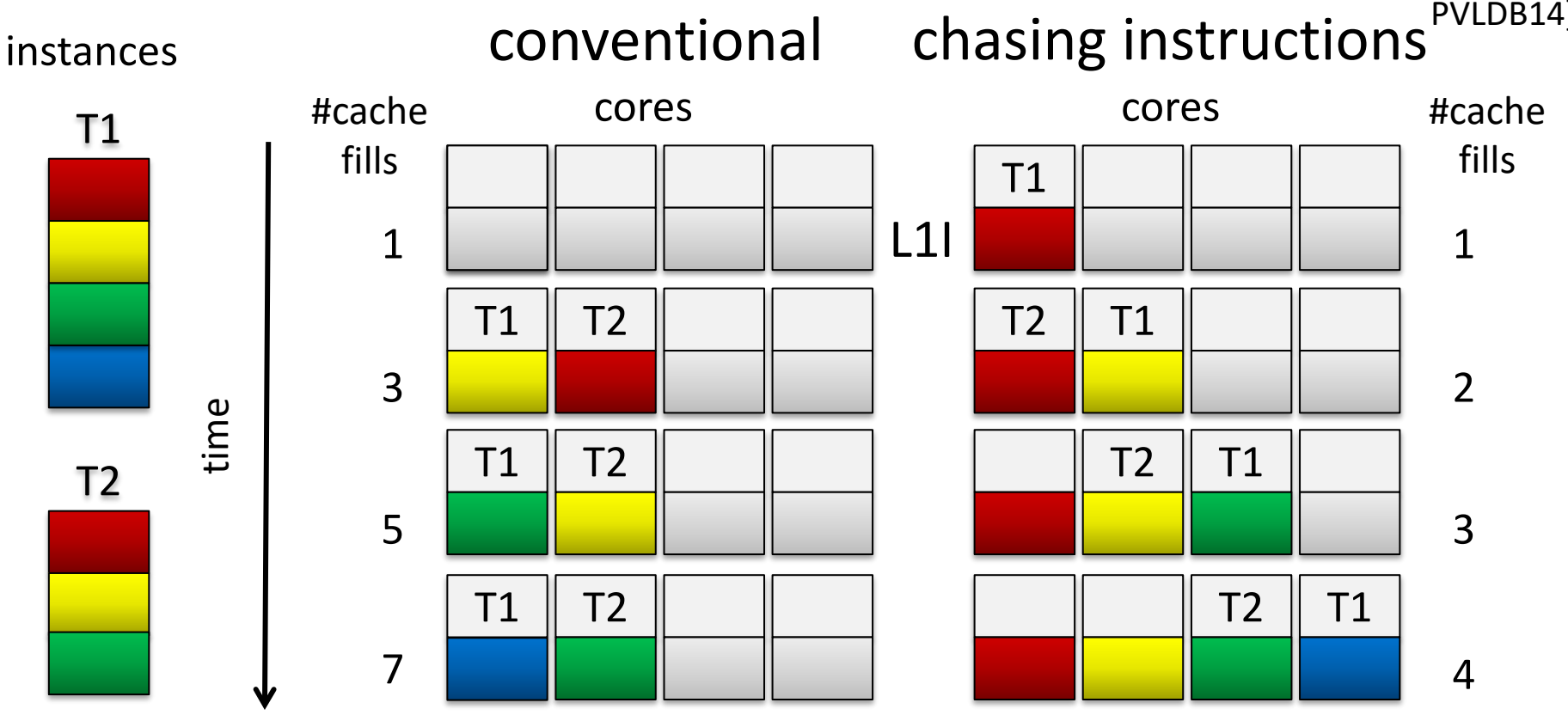
TPC-C (100GB data) on Shore-MT
overlapping cache blocks



high for instructions, low for data

exploiting instruction commonality

[MICRO12, ISCA13, PVLDB14]



can be software/hardware managed

up to 2X throughput of conventional on TPC-B/C/E

summary: OLTP & implicit parallelism

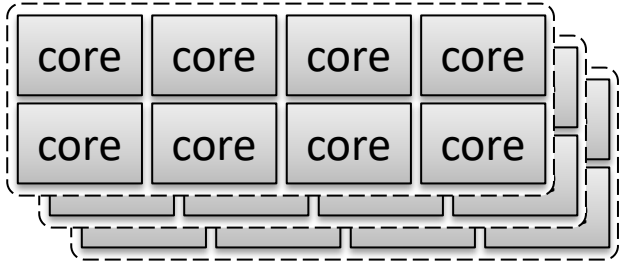
- implicit parallelism isn't completely free lunch
- >50% of cycles are stalls for traditional OLTP
  - L1-I misses are significant
- Invest in
  - utilizing instruction overlap across transactions & aggregate L1-I cache capacity
  - simplified code & cache-friendly data/code layouts that favor hardware prefetchers

agenda

- types of hardware parallelism
- implicit parallelism
- **explicit parallelism**

scaling-up vs scaling-out

scaling-up



adding more cores in a single server should give proportional performance increase

scaling-out

adding more servers in a data center should give proportional performance increase

for regular folk!

scaling-up vs scaling-out

scaling-up

adding more servers in a data center should give proportional performance increase

scaling-out

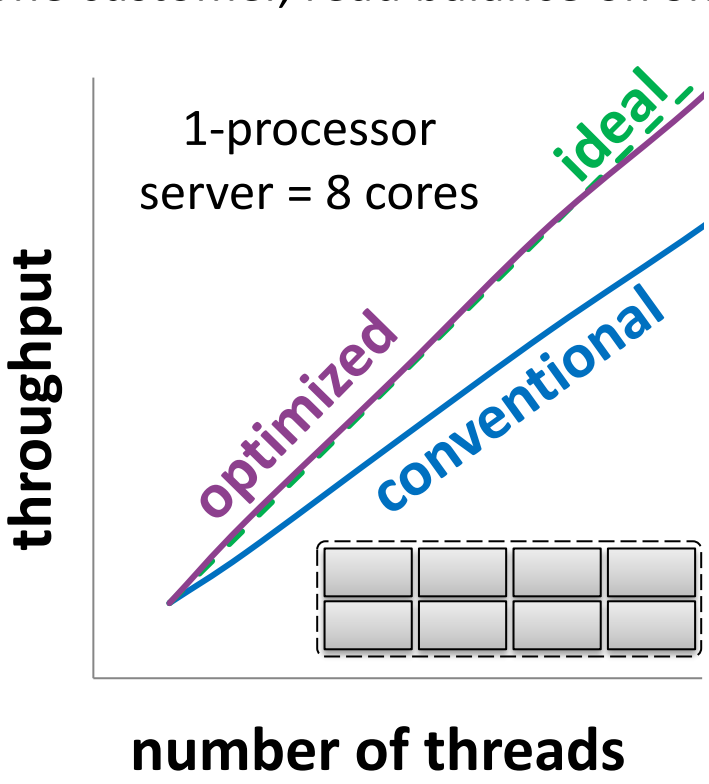
adding more data centers should give proportional performance increase

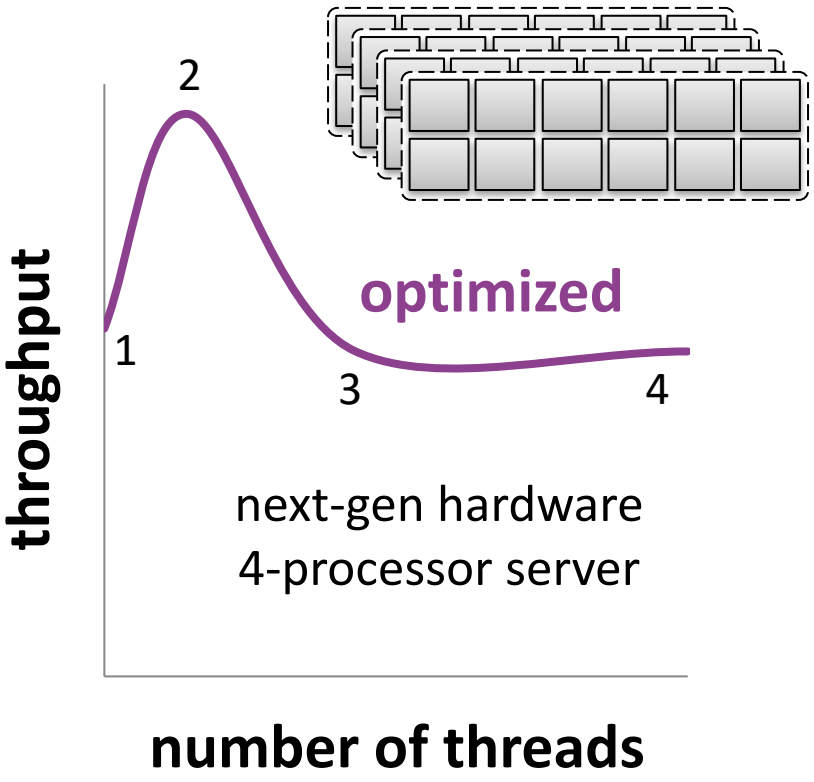
for google, amazon …!

scaling-up

[PVLDB11, PVLDB12, ICDE14]

probe one customer, read balance on Shore-MT



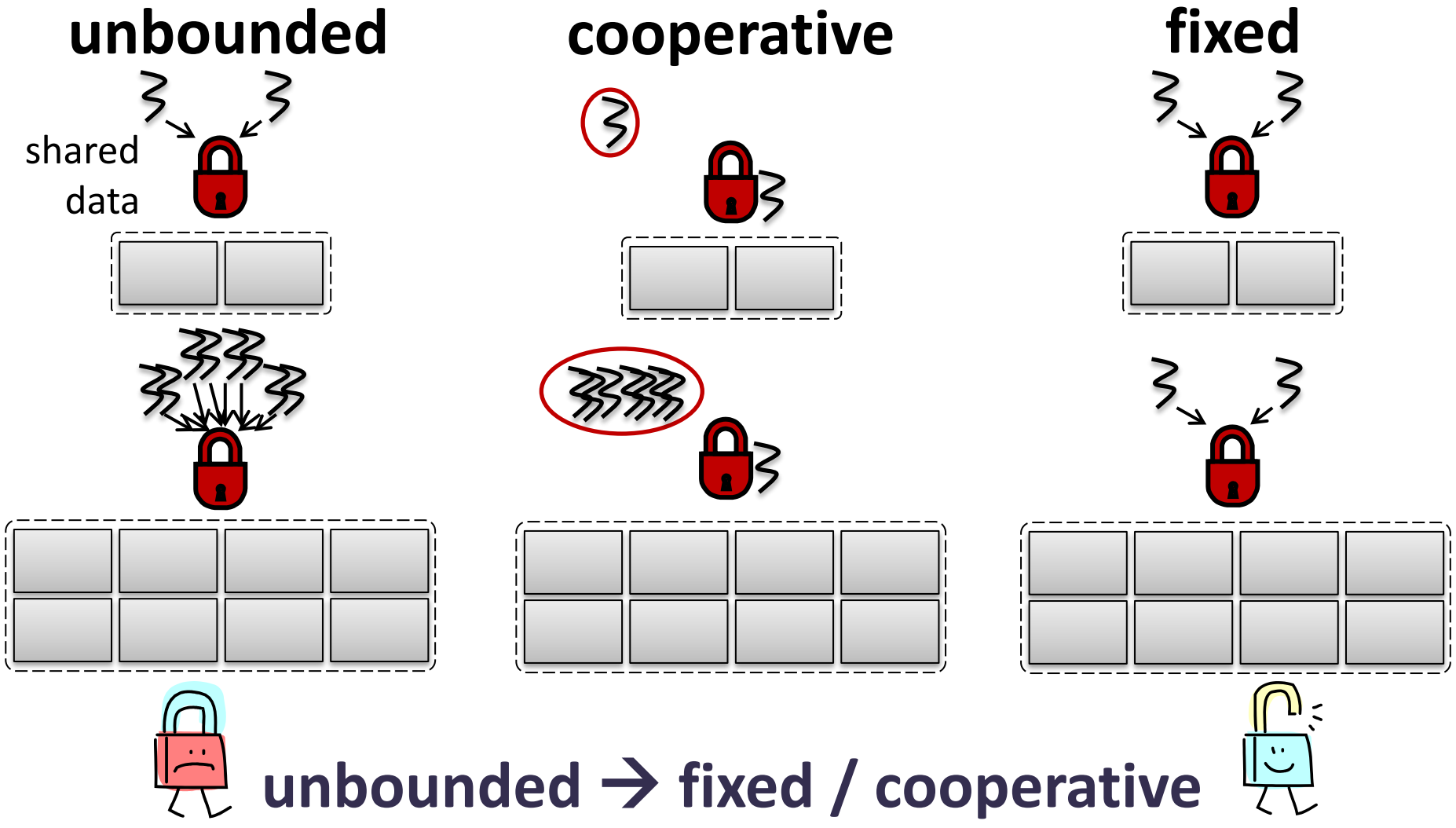


need better metrics to reason about scalability

throughput measurements are not enough

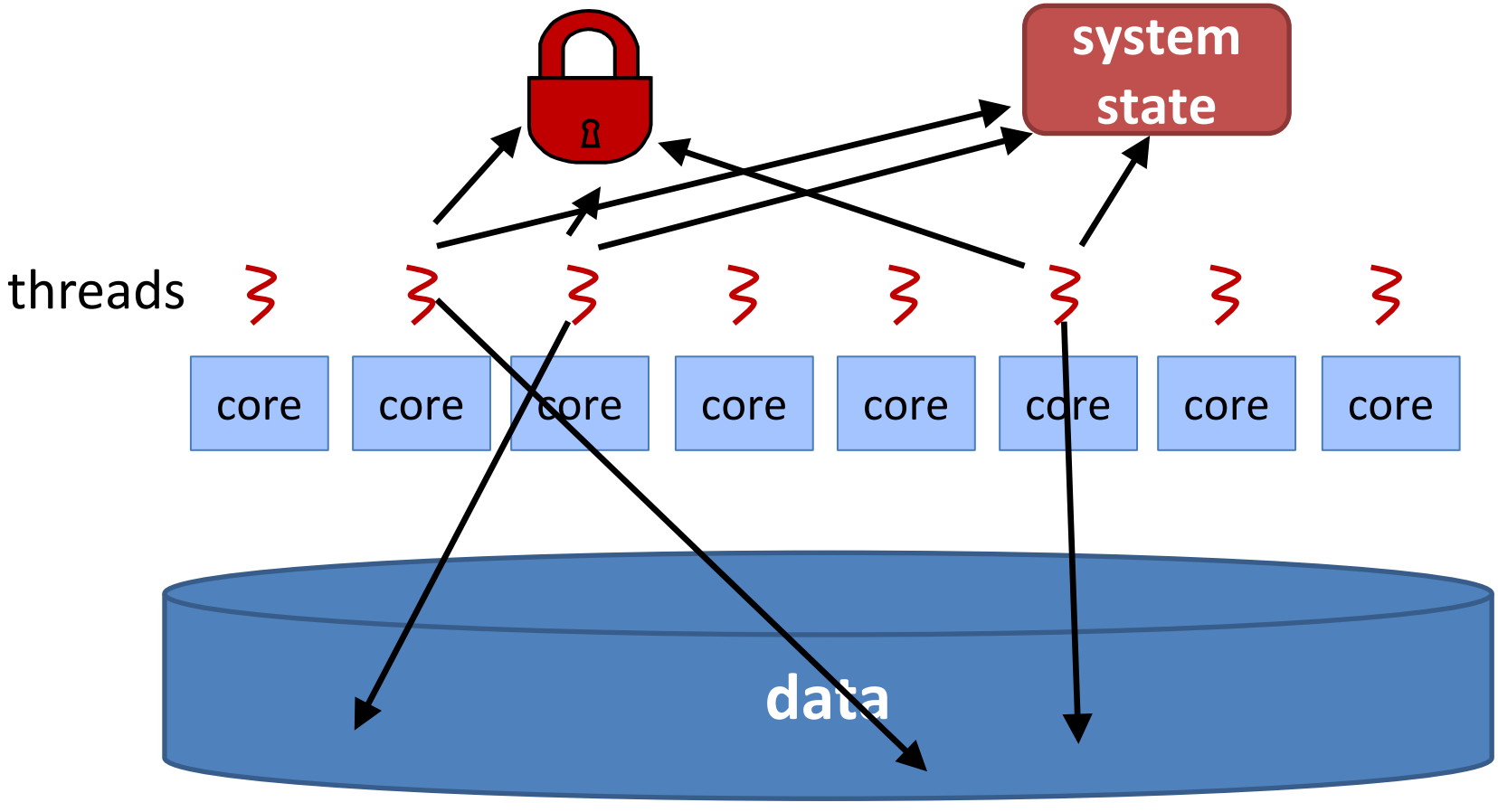
critical sections / synchronization

[PVLDB11]



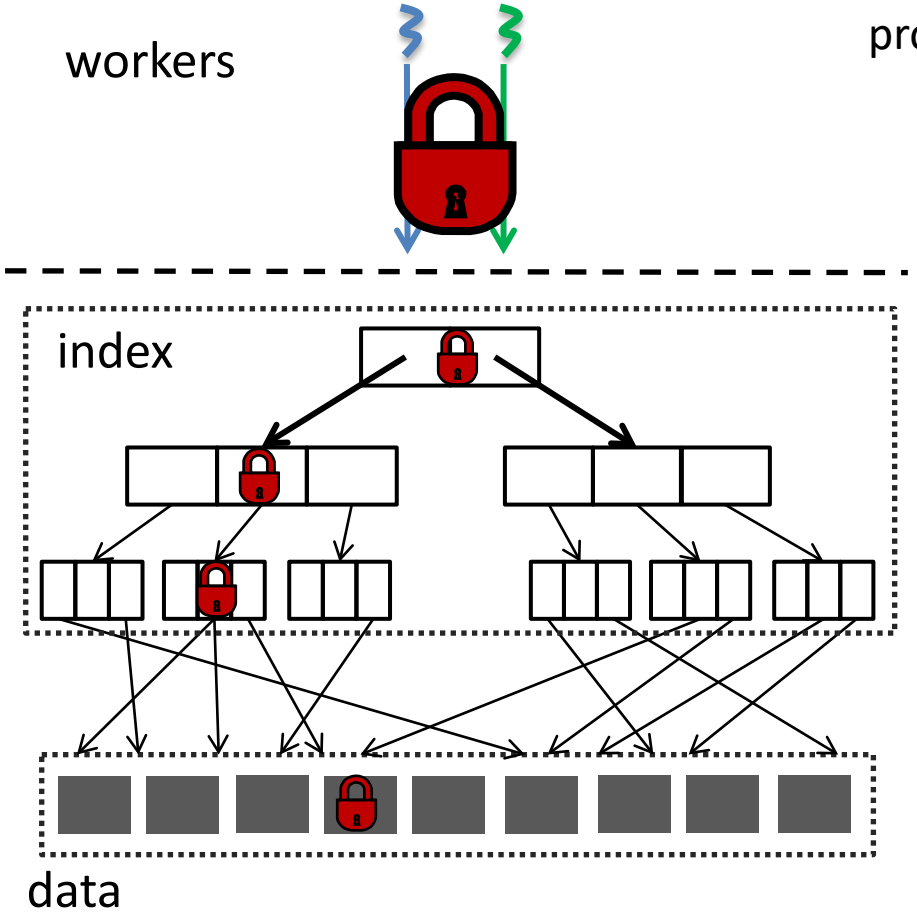
unbounded → fixed / cooperative

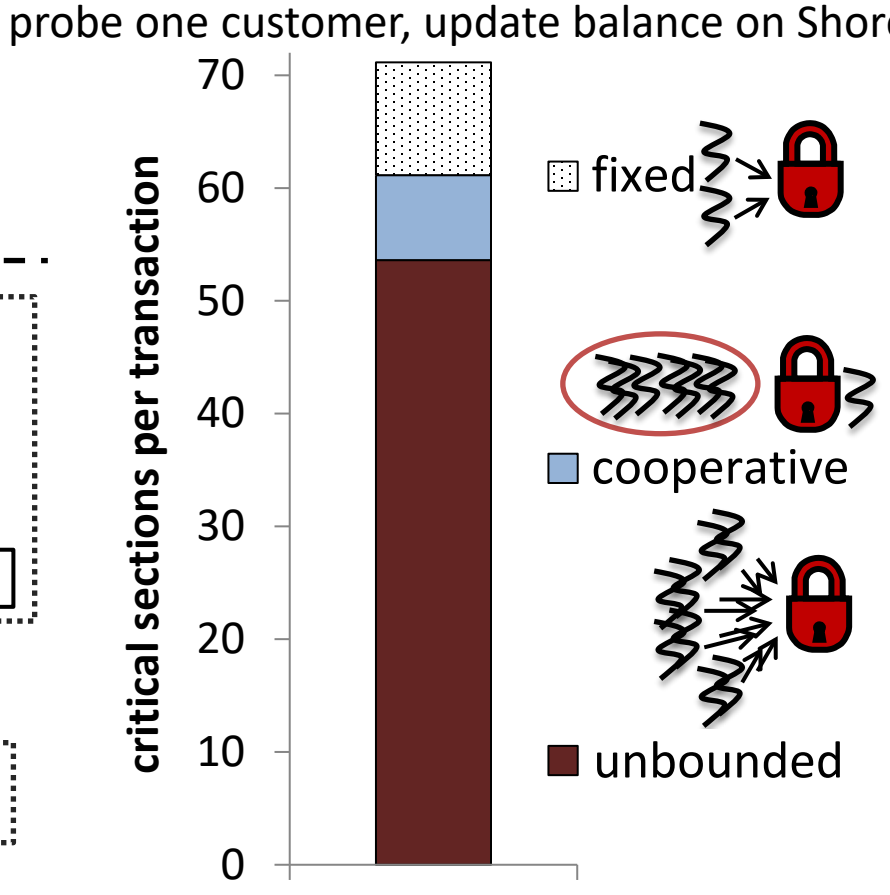
critical path of transaction execution



many unpredictable accesses to shared data

impact of unpredictable data accesses

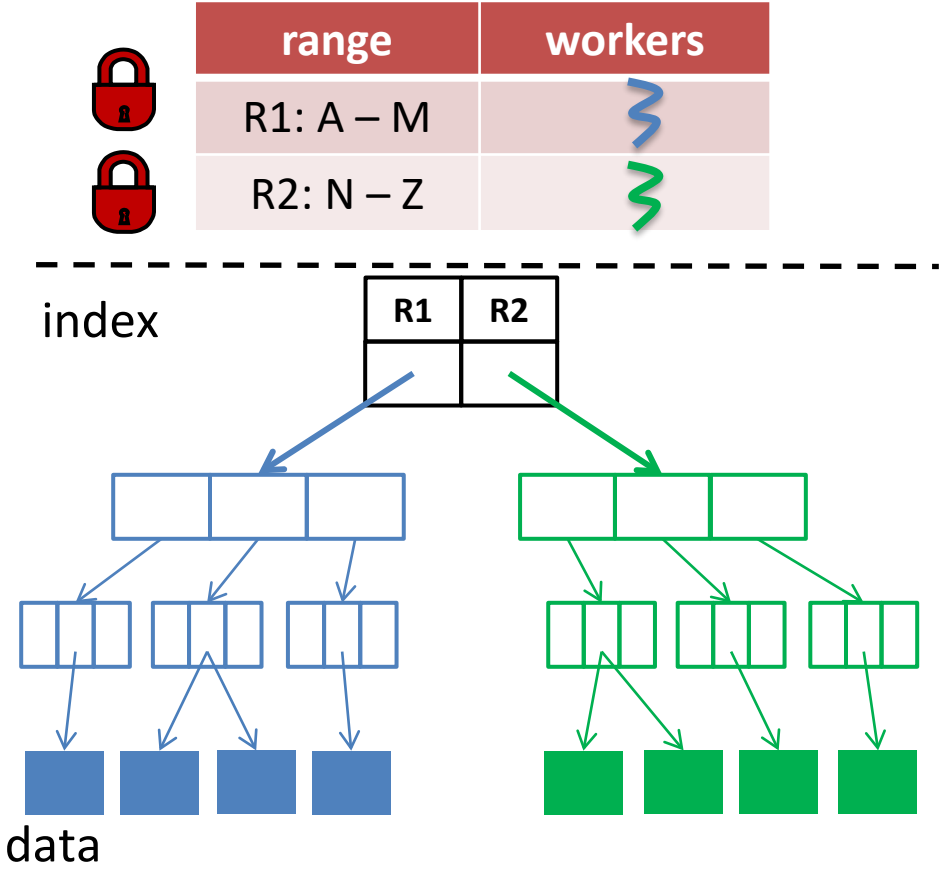


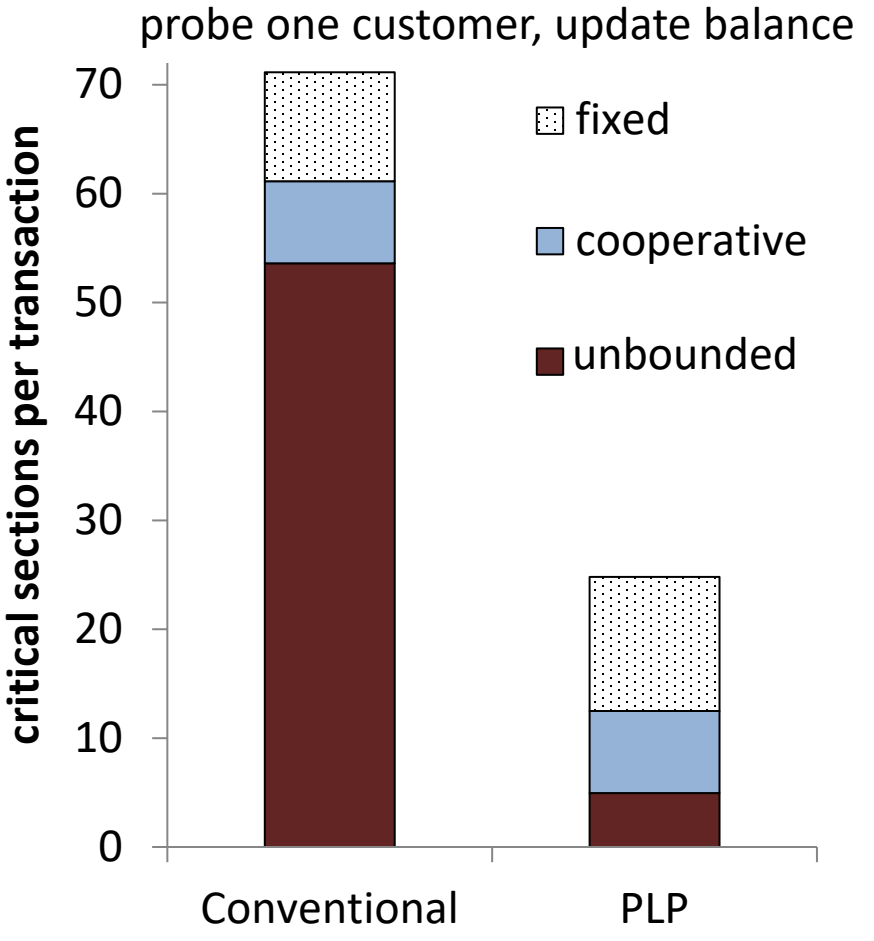


75% of critical sections are unbounded

physiological partitioning (PLP)

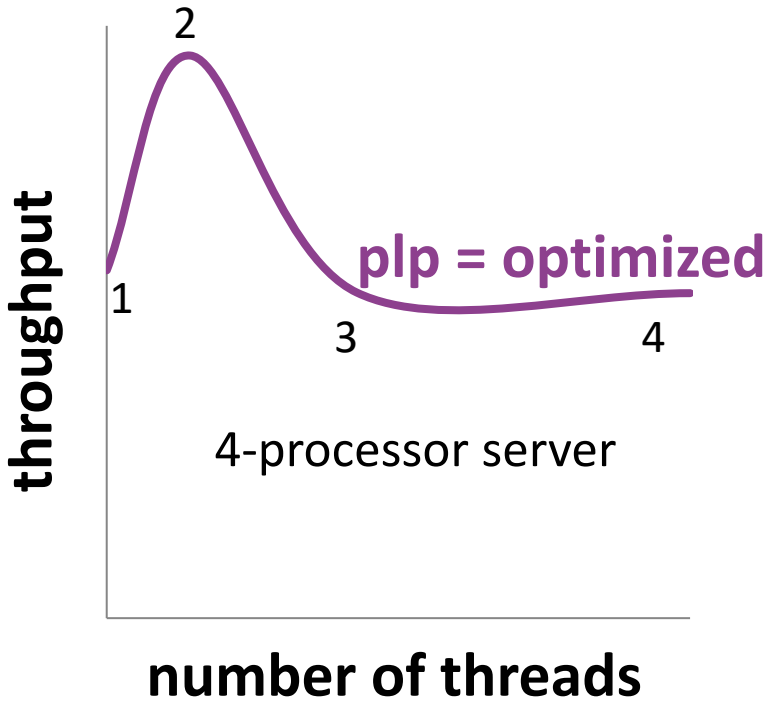
[PVLDB11]

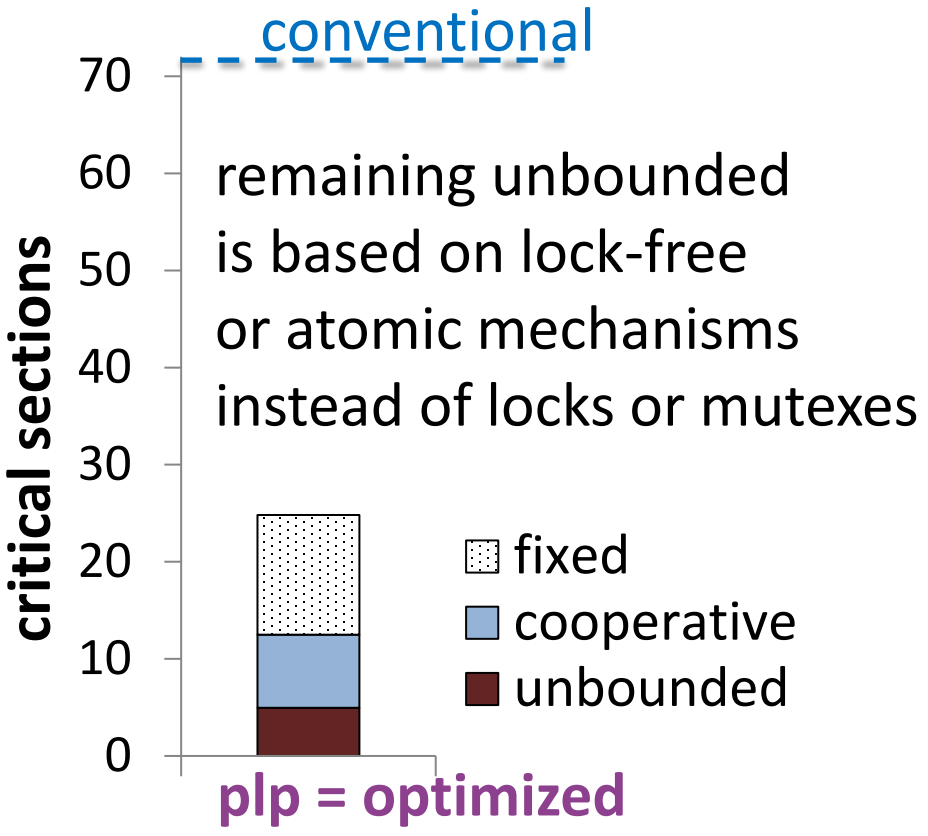




PLP eliminates 70% of critical sections

critical sections as a metric?

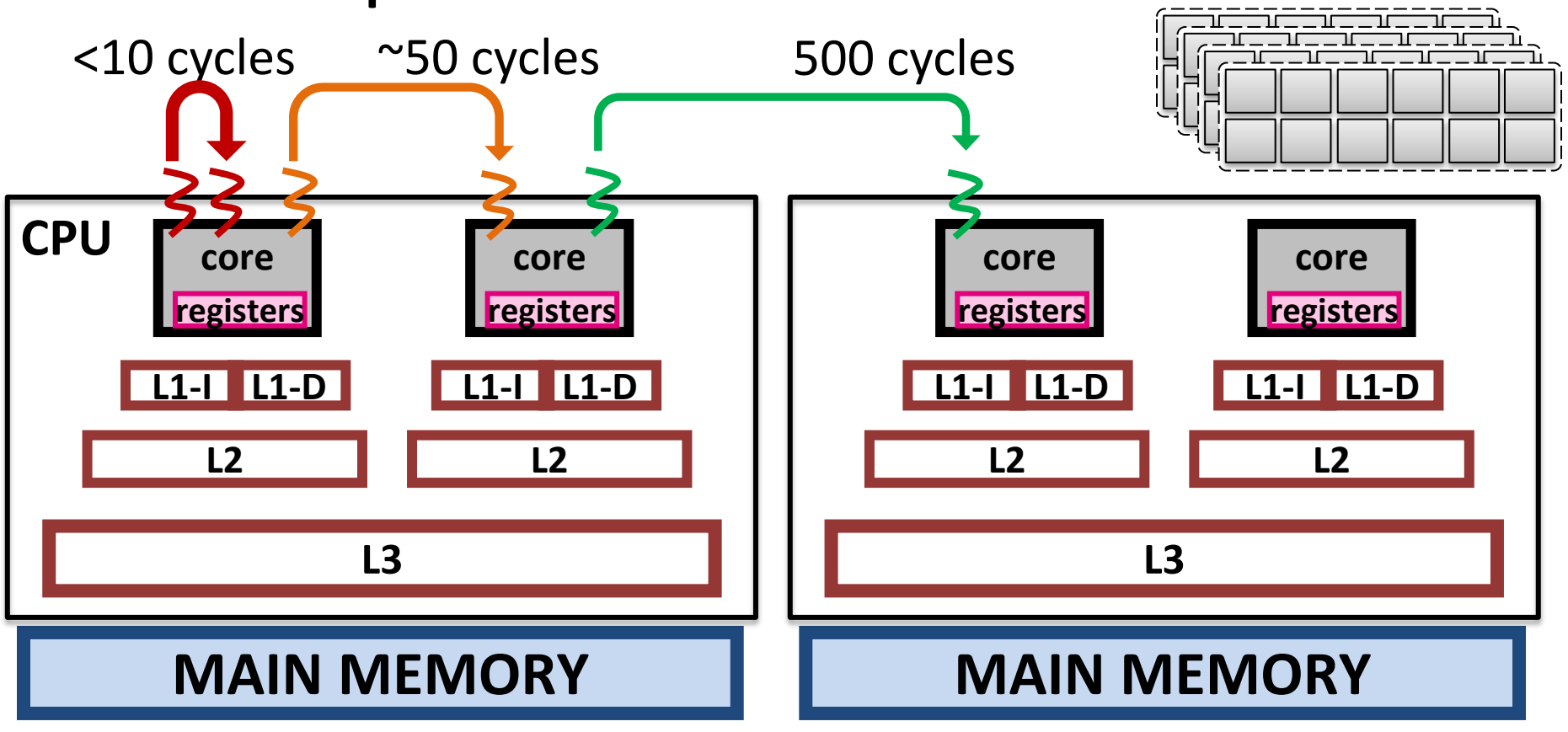




unbounded communication will hit you eventually

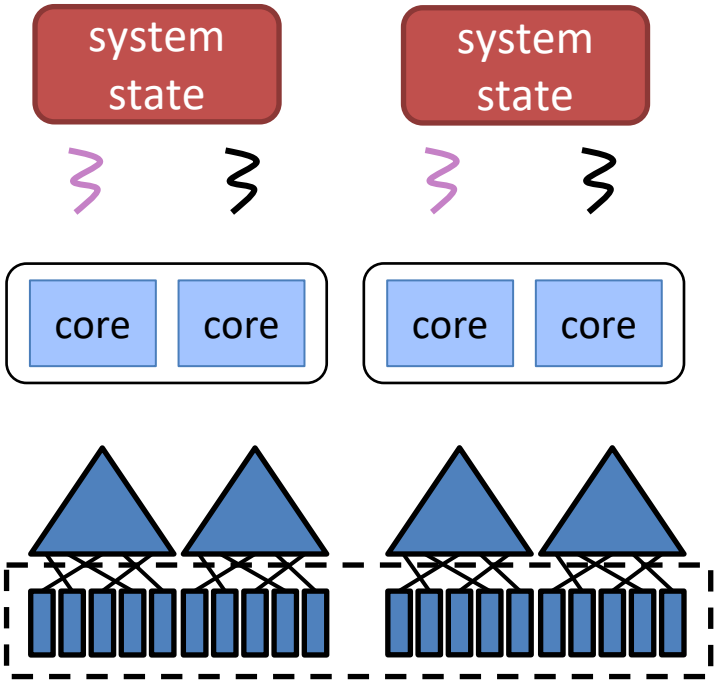
with NUMA even fixed/cooperative have issues

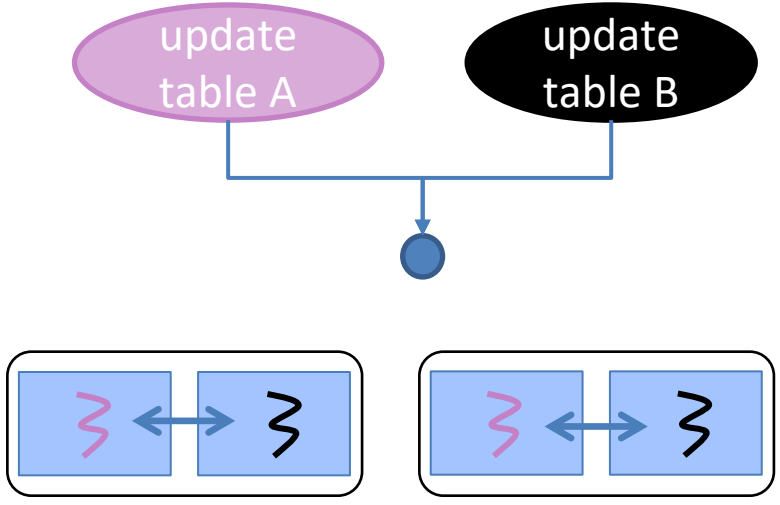
NUMA impact


<10 cycles
~50 cycles
500 cycles
CPU
core
registers
core
registers
core
registers
core
registers
L1-I
L1-D
L1-I
L1-D
L1-I
L1-D
L1-I
L1-D
L2
L2
L2
L2
L3
L3
MAIN MEMORY
MAIN MEMORY
PERSISTENT STORAGE

ATraPos: NUMA-aware PLP

[ICDE14]

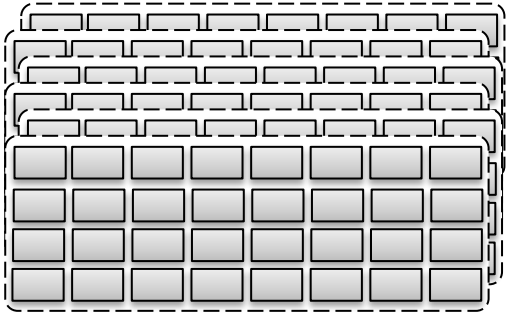




limit unbounded communication within a socket

keep access latencies predictable

summary: OLTP & explicit parallelism

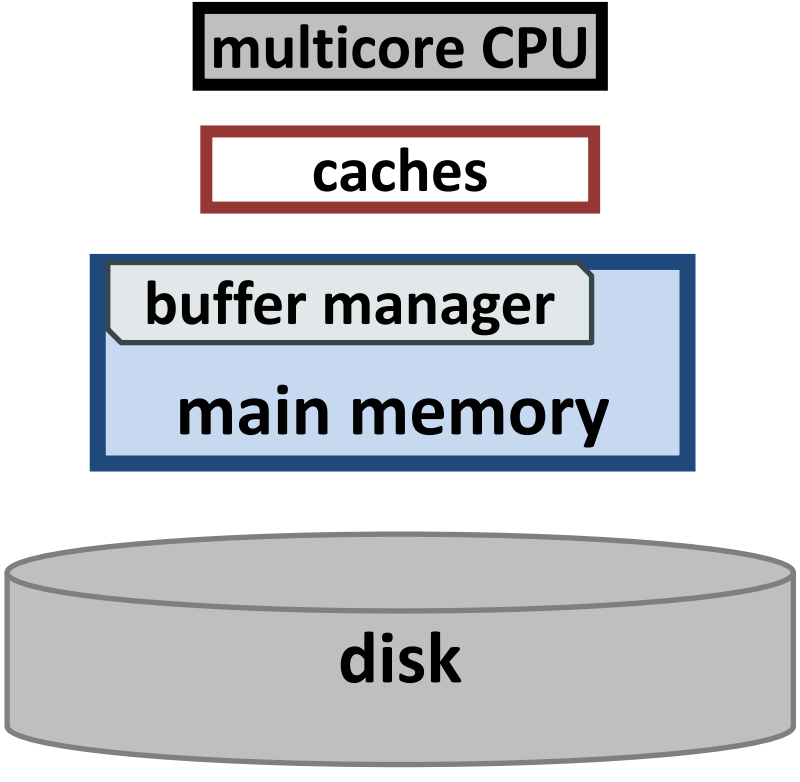


- **high throughput != scalable**
- **lock freedom != scalable**
- eliminate any unbounded communication
- keep fixed/cooperative communication among cores with similar/predictable access latency

  → avoid sharing data among cores on different processors, share within a processor (i.e., avoid NUMA impact)

today: traditional vs. modern OLTP

traditional

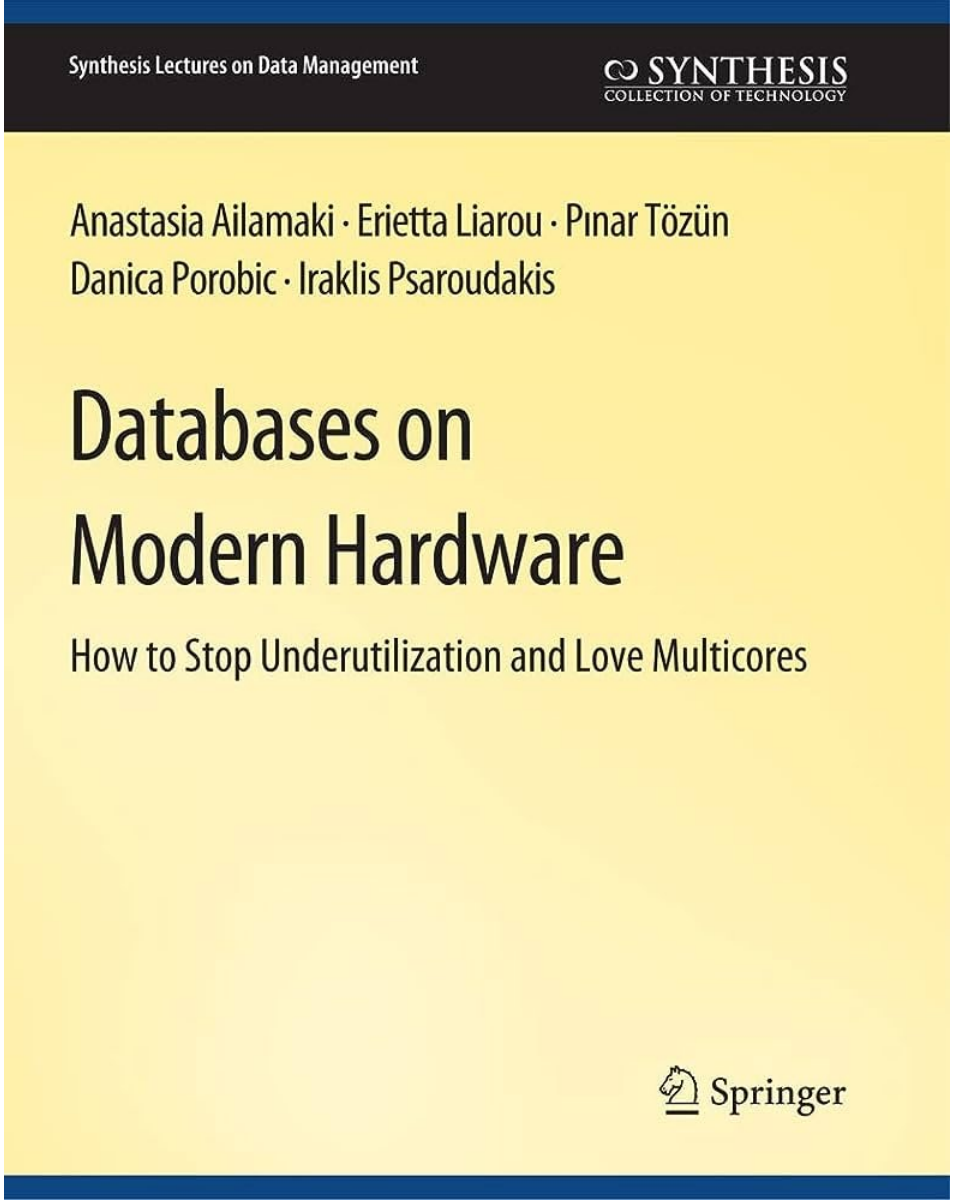


main-memory-optimized

- non-blocking concurrency control
- query compilation that generates more efficient code

- no/light buffer manager
- data organized for better cache utilization/accesses

- no disk use during analytical queries or transactions
- lightweight logging & replication for recovery
- optimize for SSDs instead


Synthesis Lectures on Data Management
SYNTHESIS
COLLECTION OF TECHNOLOGY
Anastasia Ailamaki · Erietta Liarou · Pınar Tözün
Danica Porobic · Iraklis Psaroudakis
Databases on
Modern Hardware
How to Stop Underutilization and Love Multicores
Springer

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slides 16-17, 19-20, & 22-23 are adopted from Erietta Liarou's slides for our ICDE15 tutorial
slide 37 & 41-42 are adopted from Danica Porobic's slides from ICDE14

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backup

kicking of the discussion

- to partition or not to partition?
  - lightweight locks & concurrency control still doesn't prevent unbounded communication
  - even if you don't go strict partitioning route, you need some partitioning to limit unbounded communication

- transaction processing & hardware accelerators?
  - Dennard scaling still doesn't hold
  - economies of scale also doesn't hold
  - hardware specialization is inevitable

- in-memory-optimized vs. SSD-optimized ?

summary: hardware parallelism

Hardware gives different parallelism opportunities.

Software systems used to be ignorant of this parallelism because it used to be mainly implicit.

Today, systems do not have this luxury because we have more and more explicit parallelism.

In the future, this parallelism will also increasingly be provided by heterogeneous processing units.

goal: design systems that are aware of the hardware parallelism (ideally all types of it) & its implications!

main-memory database systems

some downsides

startups/restarts are expensive

- need to load everything in-memory
- indexes has to be rebuilt
- recovery takes longer if not done carefully

could be expensive to store all data in memory

- most main-memory systems later added support for efficiently accessing cold data from disk
- today, more & more SSD-optimized systems instead

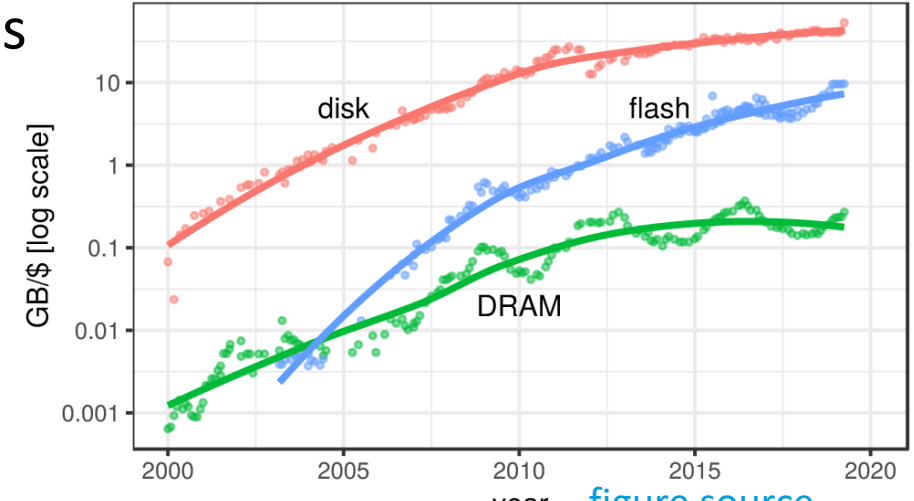


figure source

micro-architecture of an OoO processor core

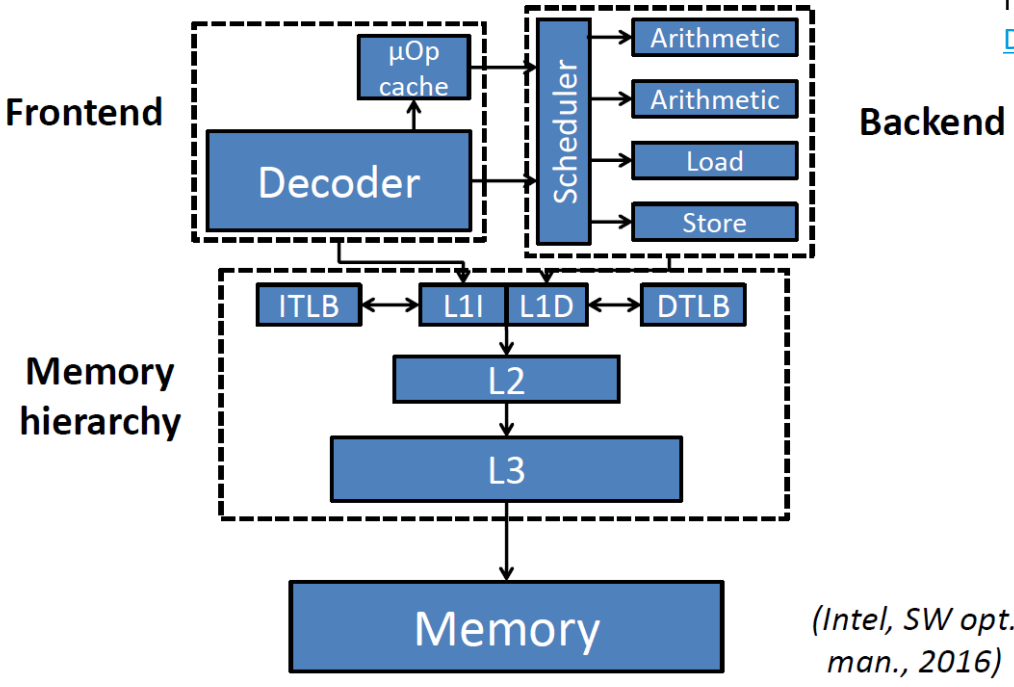


figure from Utku Şirin's DaMoN 2017 presentation

(Intel, SW opt. man., 2016)

delays in fetching, decoding, etc. an instruction cause *frontend stalls*, rest cause *backend stalls*

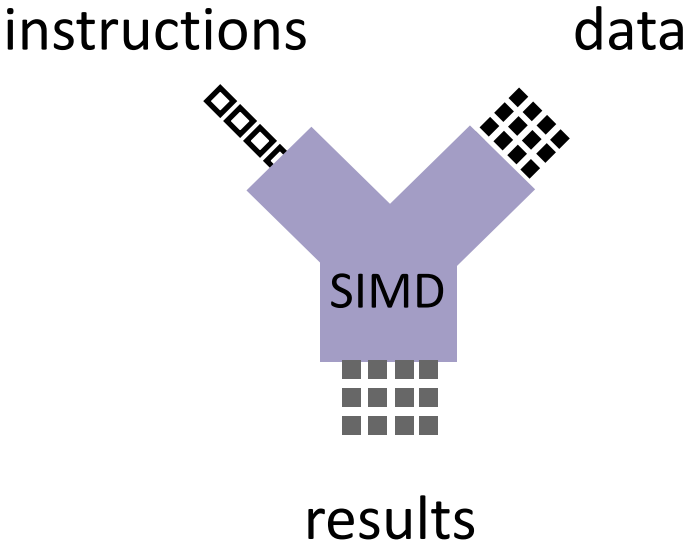
what else can be done?

- simplified code
  - newer in-memory-optimized systems have a smaller instruction footprint compared to traditional disk-based ones
- better code layout
  - minimize jumps → better utilizing hardware prefetchers
  - profiler-guided optimizations (static)
  - just-in-time (dynamic) [CIDR15]
- better code compilation
  - e.g., HyPer, Umbra, Hekaton, MemSQL
- improving index layouts → for data access efficiency

single instruction multiple data (SIMD)

if you want to apply the same instructions over multiple data items

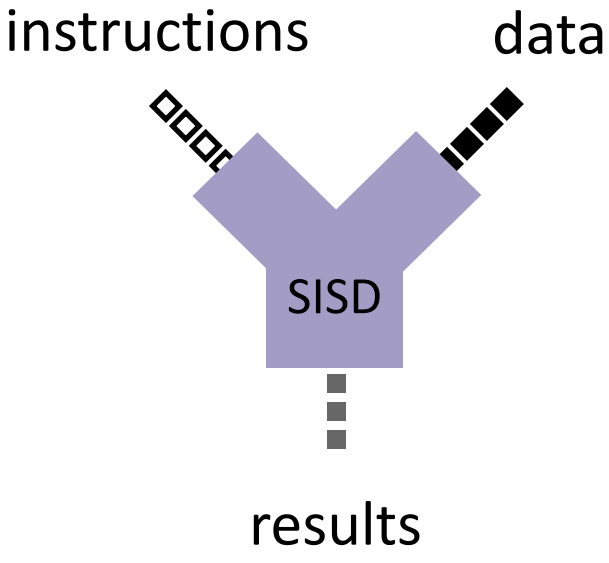
GPUs are built on this principle

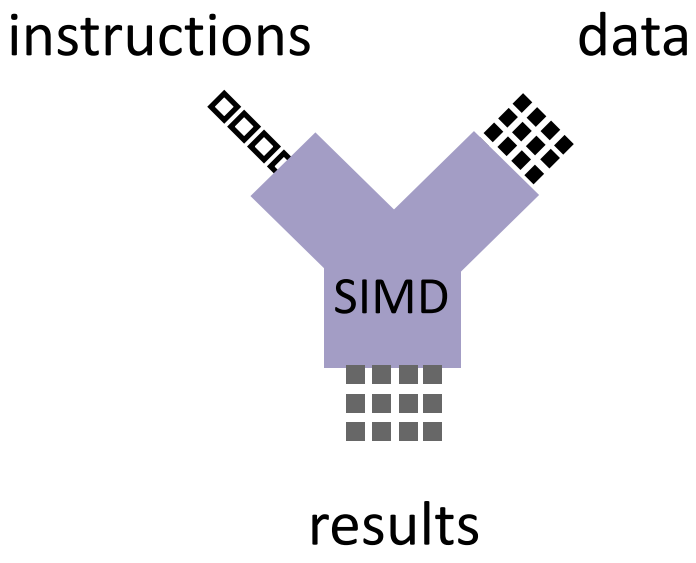


also implicit data parallelism, but this one has to be managed/issued by the software

single instruction multiple data (SIMD)

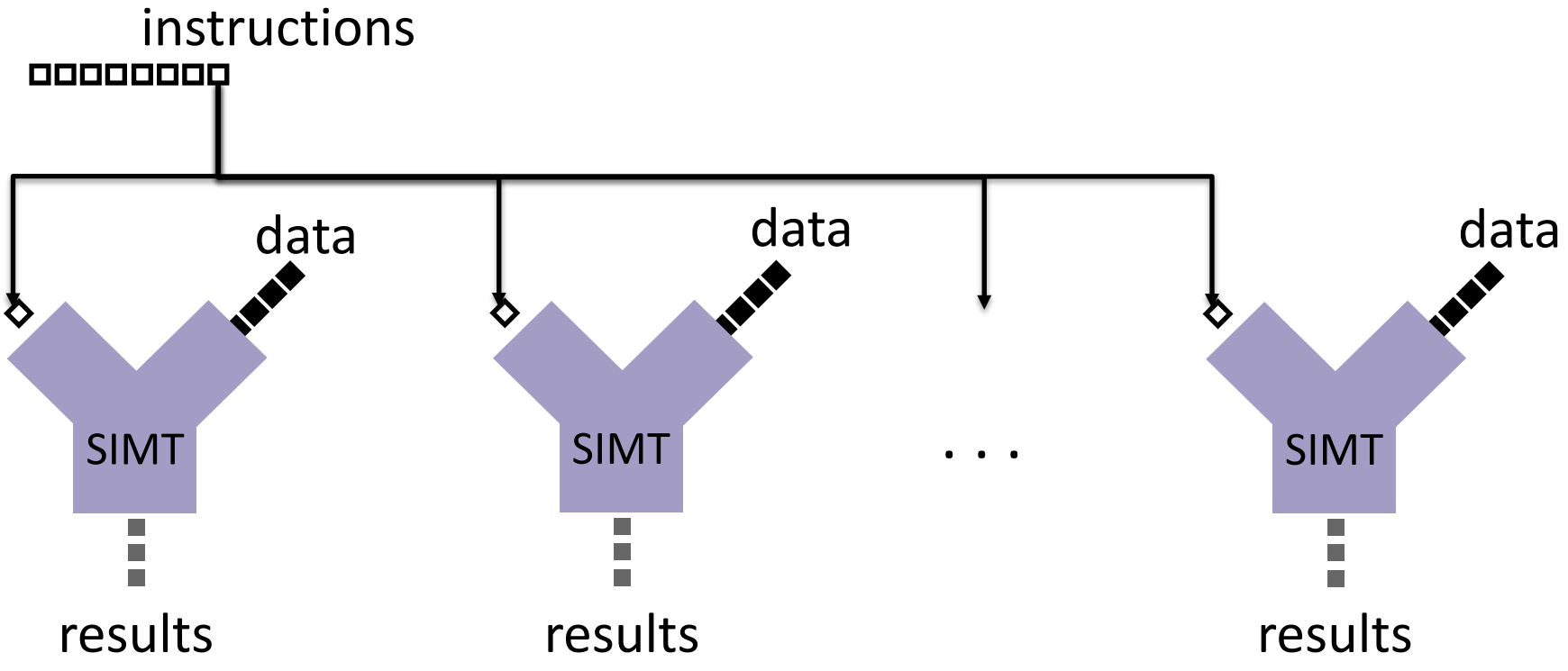
from lecture 3





GPUs are like SIMD machines
they support extreme parallelism

single instruction multiple thread (SIMT)

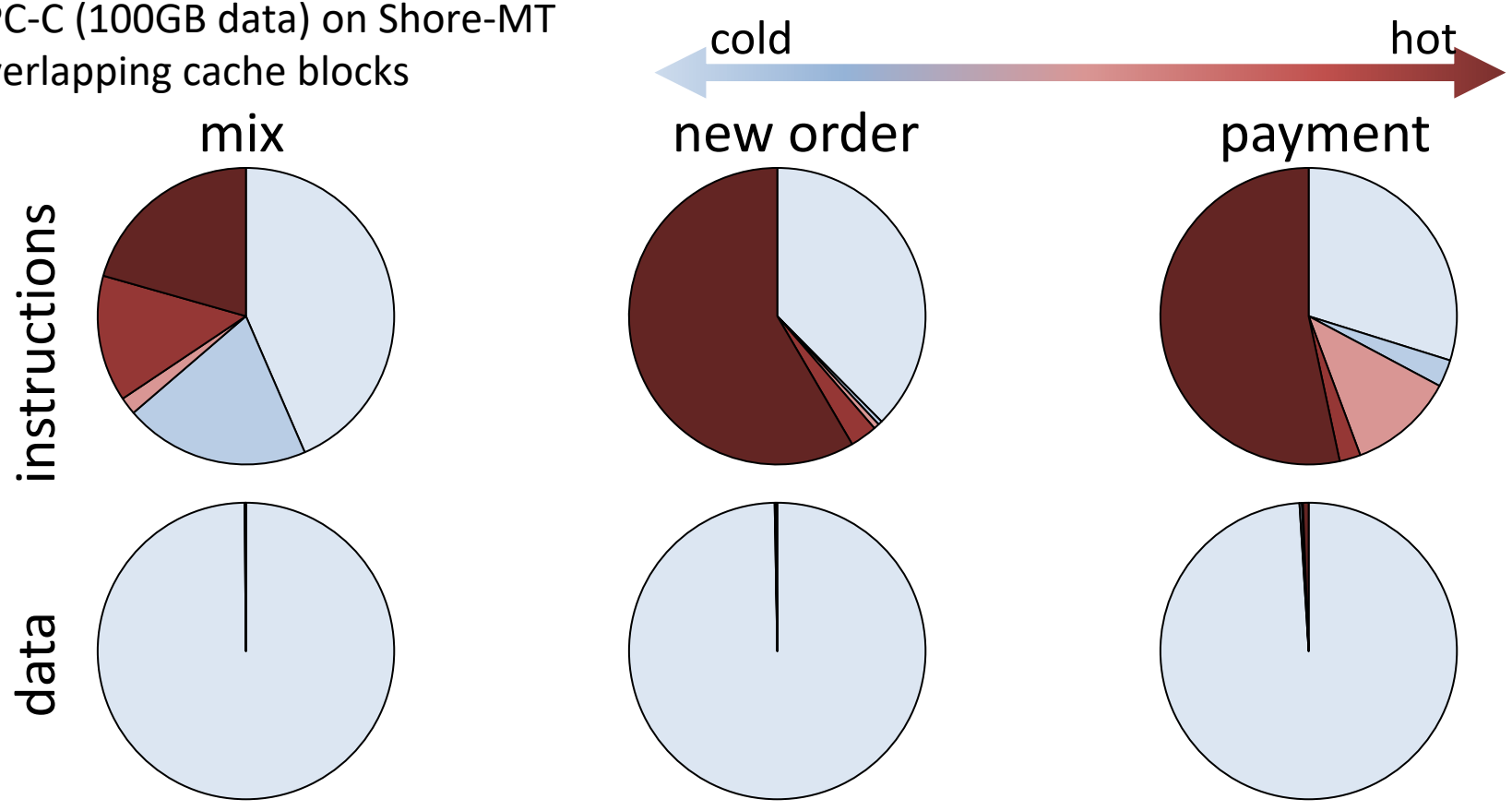


GPUs are based on SIMT

instruction & data overlap

[PVLDB14]

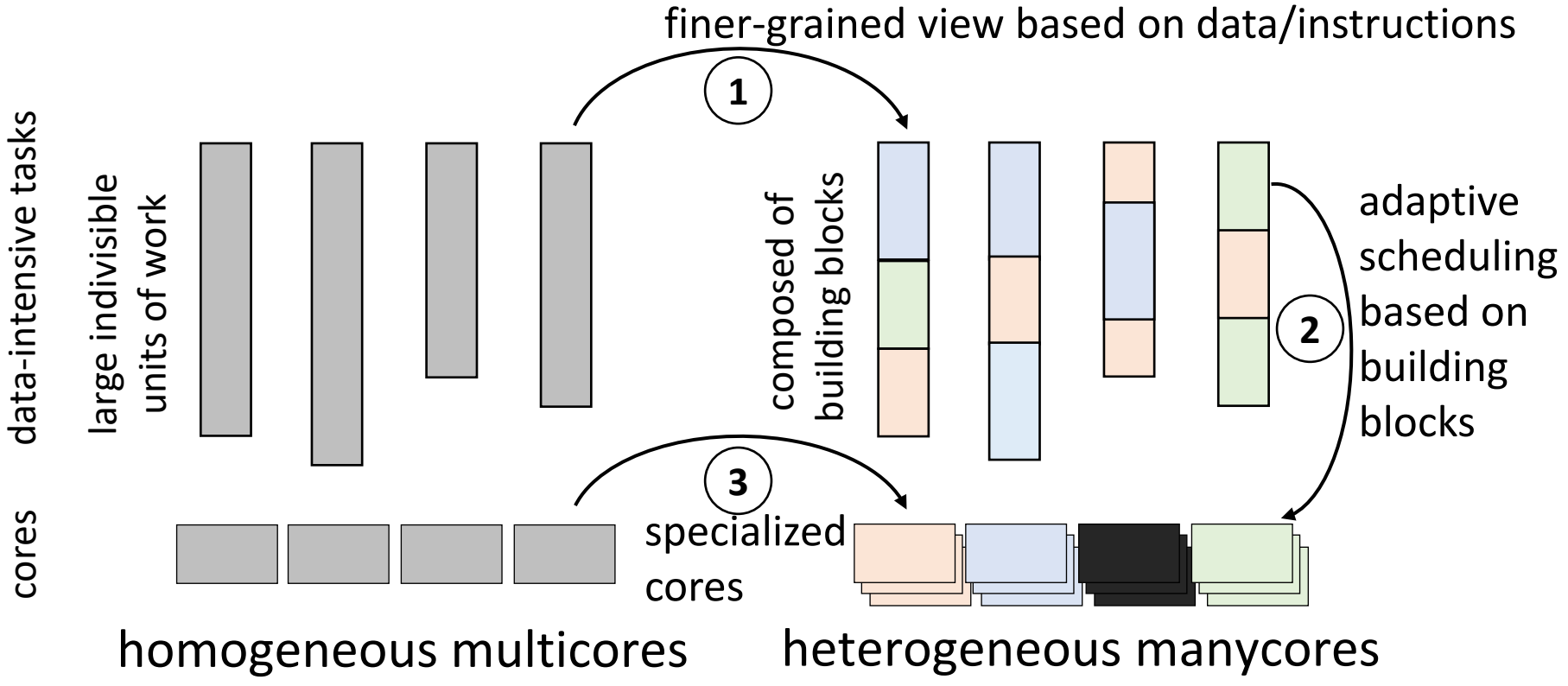
TPC-C (100GB data) on Shore-MT
overlapping cache blocks



different transaction instances are composed of common instructions

how to achieve the goal? **thank you!**

[DeBull19]



black-box view leads to sub-optimal hardware utilization

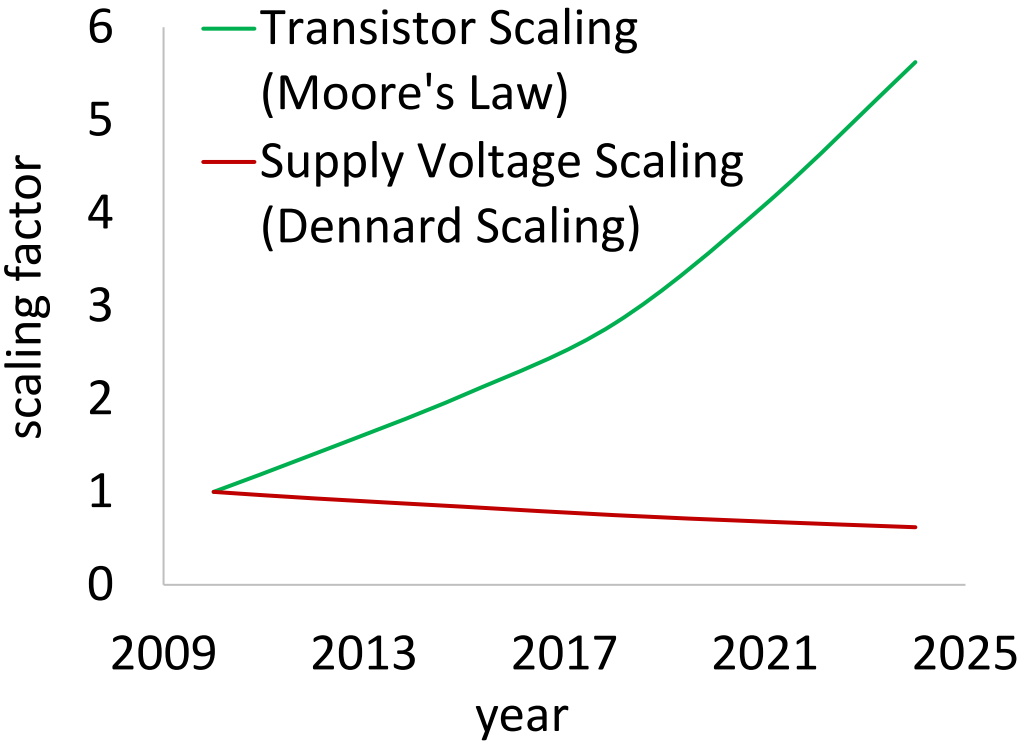
finer-grained view helps with hardware-consciousness

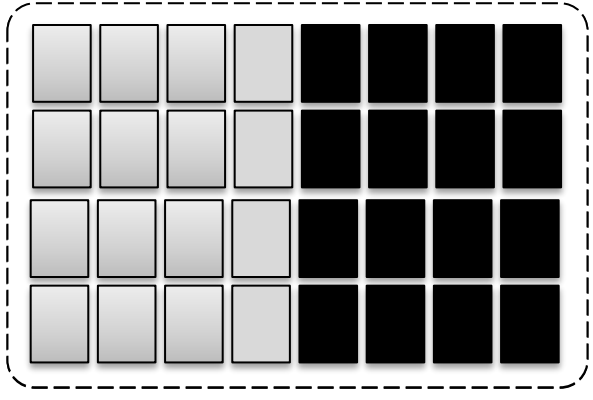
lecture agenda

- types of hardware parallelism
- implicit parallelism
- explicit parallelism
- **adding heterogeneity**

dark silicon

[ISCA11, MICRO11]



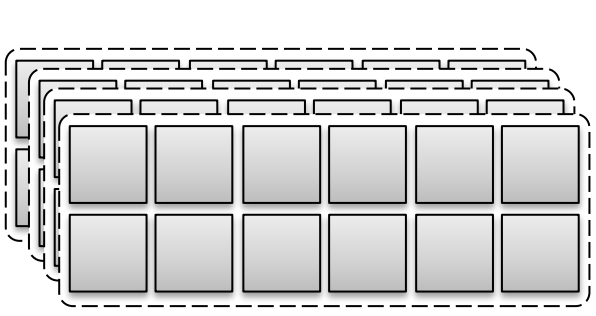


can still pack more cores in a processor

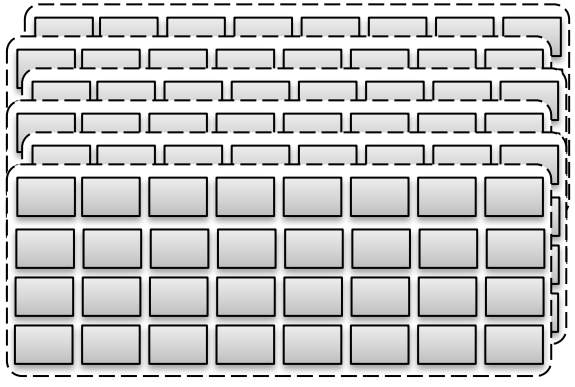
cannot fire all of them up simultaneously

what this means (for servers)

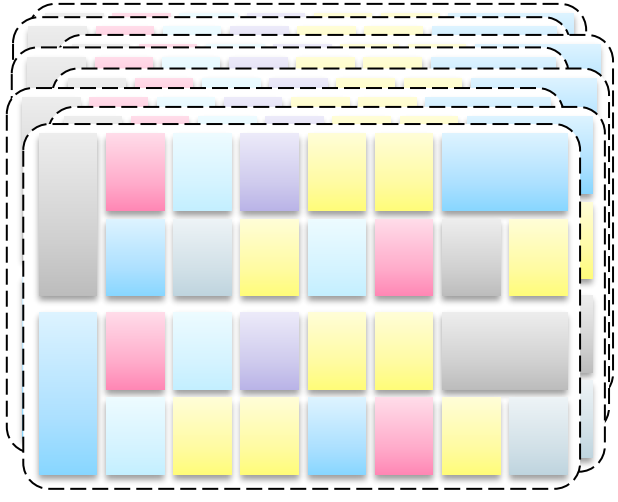
today's commodity | **future's commodity**



multisocket multicores



many (***light)*** cores



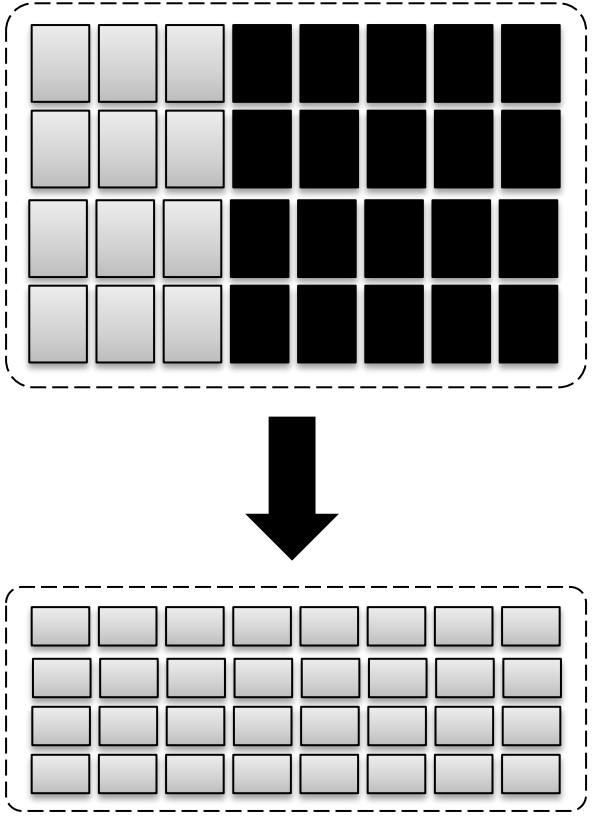
many ***diverse*** cores

more parallelism & heterogeneity

most software systems are not ready for either

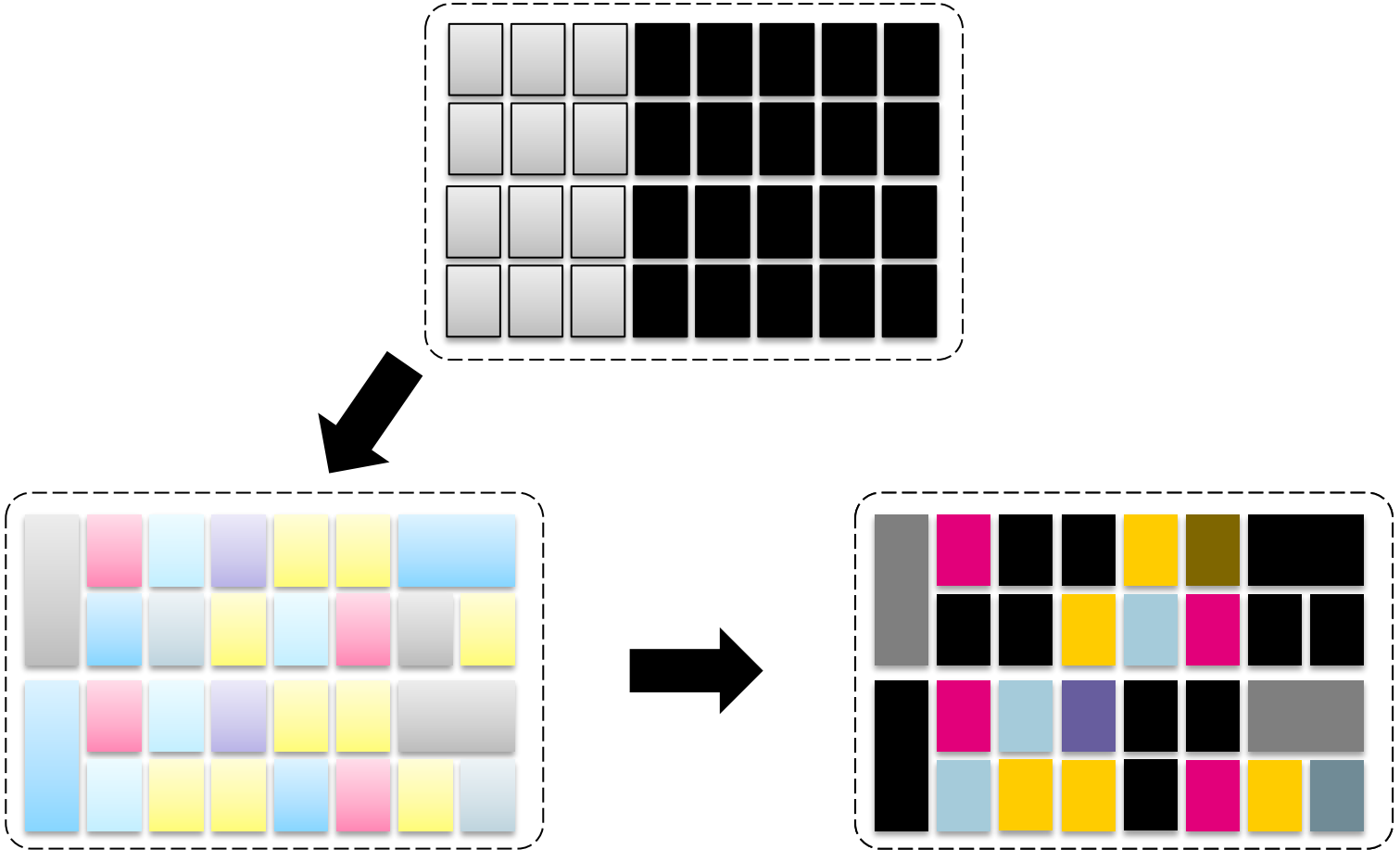
lighter cores

[MICRO10]



not feasible for latency critical tasks
can be less energy-efficient in the long run

diverse cores



better long-term solution, but creates mess

exploiting diversity

[DaMoN14, SIGMOD18a, SIGMOD18b]

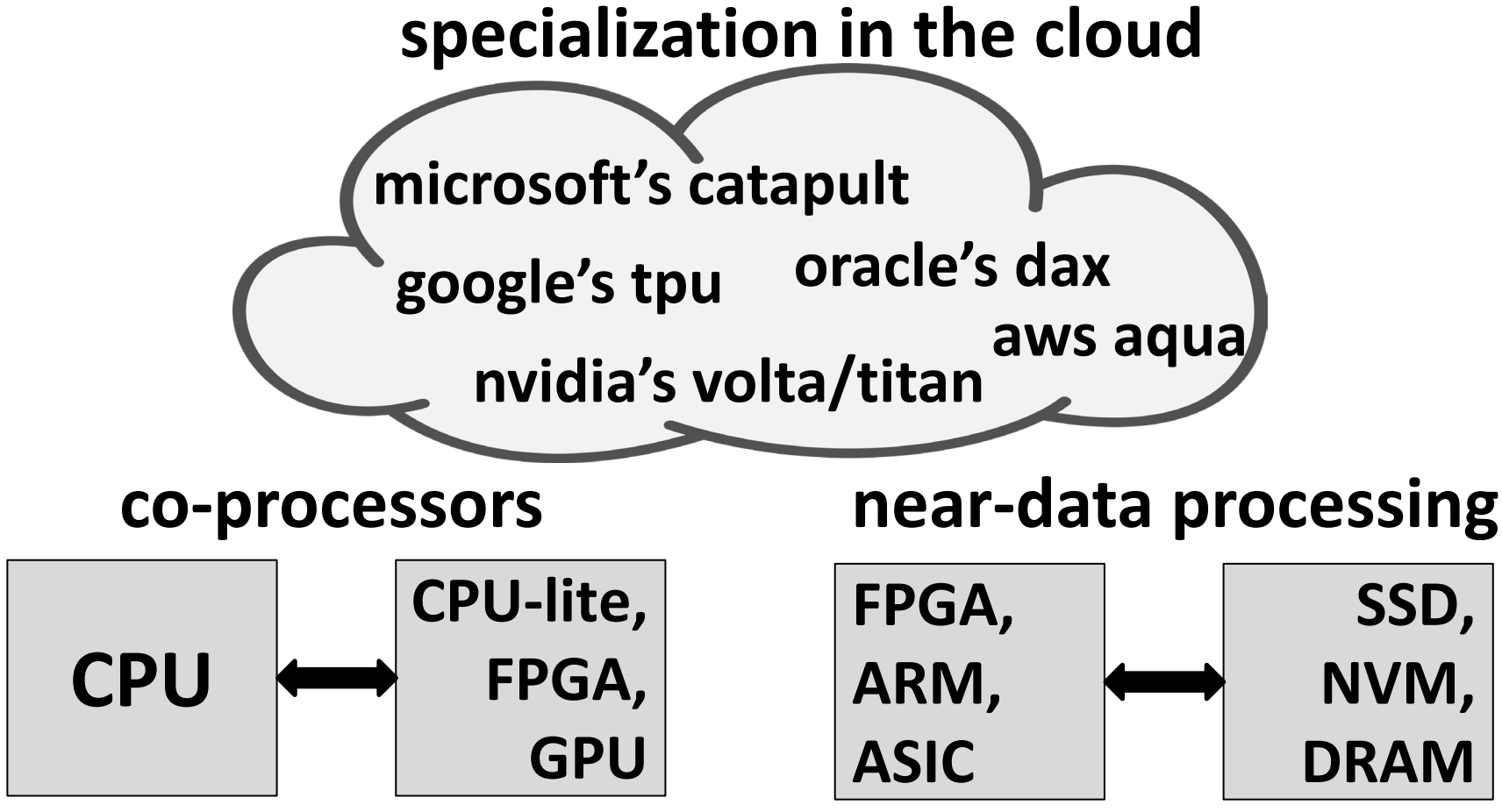
- finer-grained scheduling & energy management
  - controlling which cores are active at a time running what types of tasks & what frequency cores run on

[DEBull14, CIDR15, PVLDB16]

- language support & advanced query compilation
  - high-level languages for programs, then compile that onto different cores where instruction sets may be different

- right use case for specialization
  - must pick frequent & important tasks to accelerate – otherwise, no economic viability

today's landscape



references / credits

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